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(30)Priority

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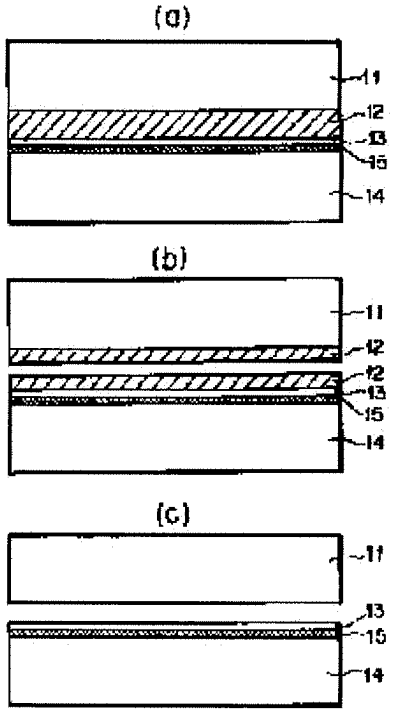
(54) SEMICONDUCTOR MEMBER AND ITS MANUFACTURE

(57)Abstract:

PROBLEM TO BE SOLVED: To simply separate a multilayer structure in a porous layer excellently.

SOLUTION: First, a first substrate 11 which has a non-porous semiconductor layer 13 formed on a porous silicon layer 12 of a silicon substrate is prepared. Next, the first substrate 11 and a second substrate 14 are stuck so as to obtain a multilayer structure wherein the non-porous semiconductor layer 13 is located inside. Then, the multilayer structure is heated to separated it in the porous silicon layer 12. Then, the porous silicon layer 12 which remains on the separated second substrate 14 side is removed and the porous silicon layer 12 which remains on the separated first substrate 11 side is also removed and the thus obtained substrates are used as raw substances for a first and a second substrate 11 and 14.



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TECHNICAL FIELD

[Field of the Invention]This invention relates to the manufacturing method of a semiconductor member including the process of transferring especially a semiconductor layer on another base (transfer) about the manufacturing method of a semiconductor member and semiconductor member for forming semiconductor devices, such as an integrated circuit, a solar cell, a semiconductor laser, a light emitting diode.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a typical sectional view for explaining the process of this invention.
[Drawing 2]It is a typical sectional view for explaining the process of this invention.
[Drawing 3]It is a typical sectional view for explaining the process of the 1st conventional example.
[Drawing 4]It is a typical sectional view for explaining the process of the 2nd conventional example.
[Description of Notations]
11 Si substrate
12 Porosity Si
13 Nonvesicular thin film
14 The 2nd substrate
15 Insulating layer
21 Si substrate
22 Porosity Si
23 Nonvesicular thin film
24 The 2nd substrate
25 The 2nd substrate
26 Insulating layer
31 Si substrate
32 Porosity Si
33 Single crystal film
34 Supporting board
35 Insulating layer
41 Si substrate
42 Porosity Si
43 Single crystal film
44 Supporting board
45 Insulating layer

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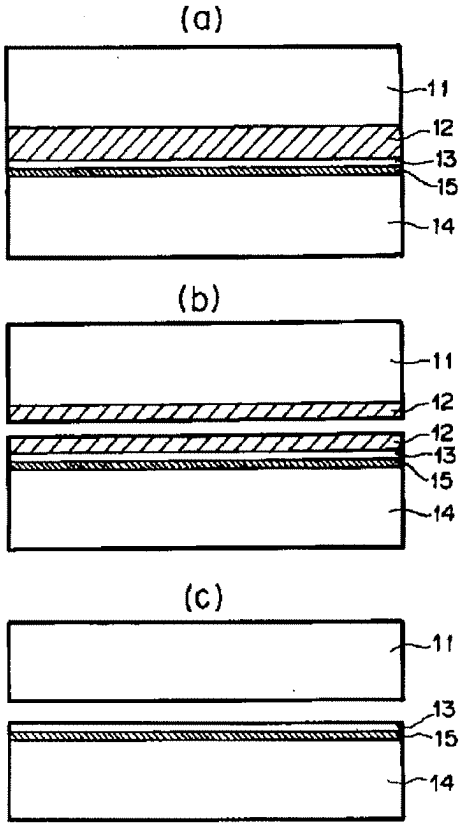
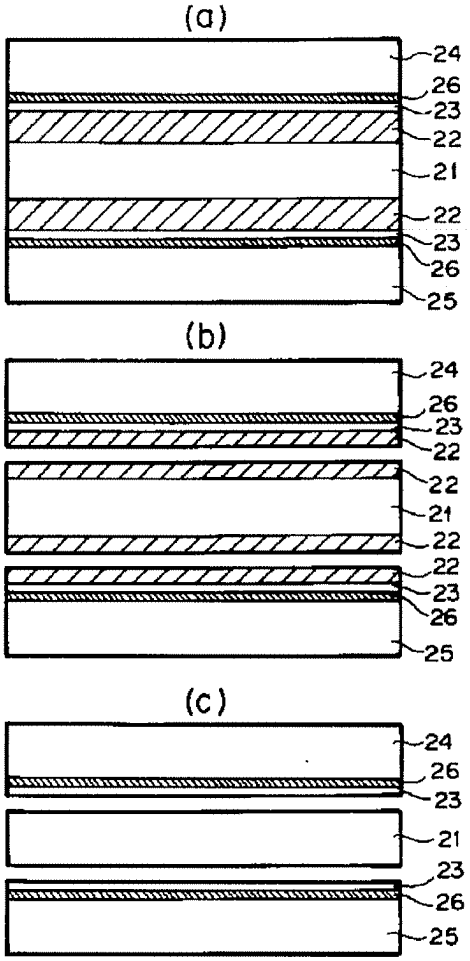
DRAWINGS

[Drawing 1]



[Drawing 2]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(b)
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(c)
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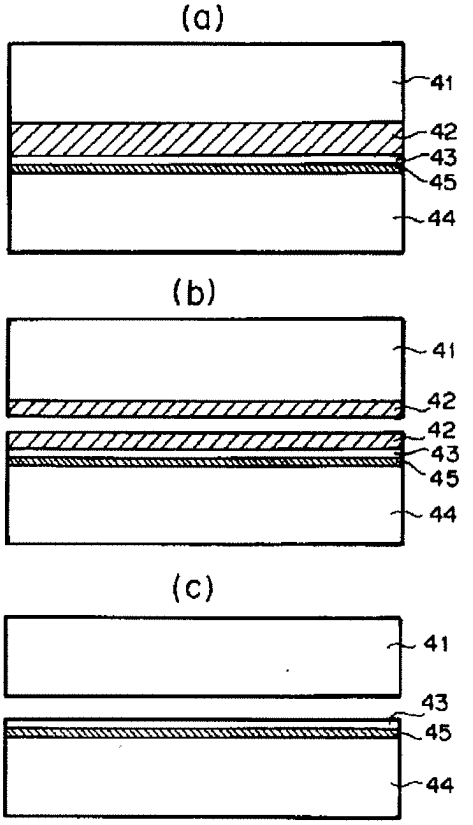
[Drawing 4]


(a)
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(b)
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(c)
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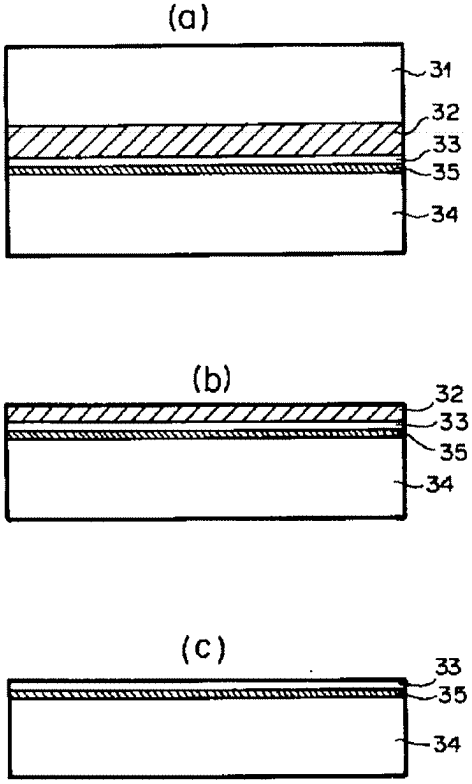
[Drawing 3]



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to the manufacturing method of a semiconductor member including the process of transferring especially a semiconductor layer on another base (transfer) about the manufacturing method of a semiconductor member and semiconductor member for forming semiconductor devices, such as an integrated circuit, a solar cell, a semiconductor laser, a light emitting diode.
[0002]
[Description of the Prior Art]The semiconductor member is known under the name of a semiconductor wafer, a semiconductor substrate, a semiconductor device, etc.
That in which the semiconductor device is formed using the semiconductor region, and the thing of the state before a semiconductor device is formed shall be included.

[0003]in such a semiconductor member, it has a semiconductor layer on an insulating material -- it is.
[0004]Formation of the single crystal Si semiconductor layer on an insulating material is silicon. One It was widely known as insulator (SOI) art, and in the bulk Si substrate which produces the usual Si integrated circuit, since the device using SOI art has many dominance points which cannot reach, many researches have accomplished. By using SOI art, 1. dielectric separation is easy and Namely, the possibility of high integration, 2. 3. stray capacitance excellent in opposite radiation resistance is reduced -- the possibility of improvement in the speed, and 4. -- a well -- the possibility of the perfect depletion type field effect transistor by the formation of 6. thin film which can prevent 5. latchup which can skip a process, and the dominance point of ** are acquired. These are detailed in the following literature. Special. Issue:. "Single-crystal silicon on non-single-crystal insulators";edited by G.W.Cullen,Journal of Crystal Growth,volume 63, no 3 and pp 429-590 (1983).
[0005]Furthermore in the past several years, many reports are made as a substrate with which MOSFET accelerates and SOI realizes low power consumption (IEEE SOI conference 1994). Since the lower part of an element has an insulating layer when SOI structure is used, as a result of being

able to simplify an isolation process compared with the case where an element is formed on a bulk Si wafer, a device process process is shortened. That is, together with highly-efficient-izing, low-pricing in total of wafer cost and process cost is expected compared with MOSFET on bulk Si, and IC.

[0006]Improvement in the speed according [perfect depletion type MOSFET] to improvement in driving force and low power consumption are expected especially. Although the threshold voltage (Vth) of MOSFET is generally determined by the impurity concentration of a channel section, in the case of perfect depletion type (FD;Fully Depleted) MOSFET using SOI, depletion layer thickness will be influenced by the thickness of SOI. Therefore, in order to build large scale integration circuit with the sufficient yield, homogeneity of SOI thickness was desired strongly.

[0007]The device on a compound semiconductor has in Si the high performance which is not obtained, for example, a high speed, luminescence, etc. Now, most of these devices grows epitaxially on compound semiconductor substrates, such as GaAs, and they are made in it. However, a compound semiconductor substrate is expensive, a mechanical strength is low, and a large area wafer has which problem with difficult production.

[0008]From such a thing, it is cheap, a mechanical strength is also high, and the trial which carries out heteroepitaxial growth of the compound semiconductor on the Si wafer which can produce a large area wafer is made.

[0009]The research on formation of a SOI substrate was prosperous from around the 1970s. The method (SOS:Sapphire on Silicon) of carrying out heteroepitaxial growth of the single crystal Si in early stages on the silicon on sapphire which is an insulating material, The method (FIPOS:Fully Isolation by Porous Oxidized Silicon) and oxygen-ion-implantation method which form SOI structure according to the dielectric separation by oxidation of porosity Si were often studied.

[0010]The FIPOS method an N type Si layer on the P type Si-single-crystal-substrate surface A proton ion implantation, (J.Crystal Growth, vol 63,547 (1983) besides Imai) -- or, After porosity-izing only a P type Si substrate by the anodization method in an HF solution so that it may form in island shape and Si island may be surrounded from the surface by epitaxial growth and patterning, it is the method of carrying out dielectric separation of the N type Si island by accelerating oxidation. In this method, Si field separated is determined before the device process, and there is a problem that the flexibility of a device design may be restricted.

[0011]An oxygen-ion-implantation method is a method called the first SIMOX to be reported by KIzumi. To a Si wafer, after carrying out 10^{17}-10^{18} / cm^2 grade pouring of the oxygen ion, it anneals at the elevated temperature of about 1320 degrees in argon and oxygen environment. As a result, the oxygen ion poured in focusing on the depth equivalent to the projection range (Rp) of an ion implantation combines with Si, and an oxidation Si layer is formed. In that case, the Si layer made amorphous by the oxygen ion implantation of the upper part of an oxidation Si layer is also recrystallized, and it becomes a single crystal Si layer. The defect contained in a surface Si layer is making the amount of placing of oxygen 10^5/cm^2 4x10^{17} / near cm^2 conventionally, although it was large, and it has succeeded in decreasing to -10^2/cm^2. However, since the range of the infused

energy which can maintain the membraneous quality of an oxidation Si layer, the crystallinity of a surface Si layer, etc., and an injection rate was narrow, the thickness of the surface Si layer and the embedding oxidation Si layer (BOX;Burried Oxide) was restricted to the specific value. In order to obtain the surface Si layer of desired thickness, sacrifice oxidation or to grow epitaxially were required. In that case, as a result of being superimposed on the degraded minute by these processes, there is a problem that thickness uniformity deteriorates in distribution of thickness.

[0012]It is reported that the formation poor field of oxidation Si where SIMOX is called a pipe exists. As one of the cause of this, foreign matters, such as dust at the time of pouring, are considered. In the portion in which a pipe exists, degradation of a device property will arise by leak between an active layer and a supporting board.

[0013]Since the ion implantation of SIMOX has many injection rates compared with the ion implantation used by the usual semiconductor process as above-mentioned, even if a device for exclusive use is developed, in addition, injection time is long. Since an ion implantation carries out the raster scan of the ion beam of a predetermined current amount, or extends a beam and is performed, increase of injection time is assumed with large-area-izing of a wafer. In the high temperature heat treatment of the large area wafer, it is pointed out that problems, such as generating of the slip by the temperature distribution in a wafer, become severeer. In SIMOX, by Si semiconductor process of 1320 **, since heat treatment in the elevated temperature which does not carry out normal use is indispensable, we are anxious about the importance of this problem becoming still larger including device development.

[0014]Apart from the formation method of the above conventional SOI, the method of using heat treatment or adhesives for another Si single crystal substrate which oxidized the Si single crystal substrate thermally, and forming lamination and SOI structure is capturing the spotlight in recent years. This method needs to thin-film-ize the active layer for a device uniformly. That is, it is necessary to thin-film-ize a Si single crystal substrate hundreds of micrometers thick to mum order or less than it. There are three kinds of methods in this thin film-ization as follows.

(1) It is difficult to thin-film-ize uniformly in the polish of thin-film-izing (1) by the thin film-ized (3). selective etching by the thin film-ized (2). partial plasma etching by . polish. Dispersion of especially thin film-ization of sub mum can also be tens of%, and this equalization poses a big problem. If large caliber-ization of a wafer furthermore progresses, the degree of difficulty will just increase.

[0015]After thin-film-izing the method of (2) by the method by polish of (1) to about 1-3 micrometers by the method of (1) beforehand, it carries out multipoint measurement of the thickness distribution on the whole surface. It etches amending thickness distribution by making the plasma using SF_6 several millimeters in diameter etc. scan based on this thickness distribution after this, and thin-film-izes to desired thickness. By this method, it is reported that thickness distribution is made to about **10 nm. However, since this foreign matter will serve as an etching mask if there is a substrate top foreign matter (particle) in the case of plasma etching, a projection will be formed on a substrate.

[0016]Since the surface is ruined immediately after etching, touch polishing is required after the end of plasma etching, but since control of the amount of polishing is performed by time management,

control of the last thickness and degradation of the thickness distribution by polishing are pointed out. Since abrasive soap, such as colloidal silica, furthermore grinds the surface which becomes an active layer directly against polish, we are anxious also about formation of the crushing layer by polish, and introduction of working distortion. Since plasma etching time increases in proportion to increase of a wafer surface product when a wafer is furthermore large-area-ized, we are anxious also about the remarkable fall of a throughput.

[0017]The method of (3) is the method of building the film constitution in which selective etching is possible to the substrate thin-film-ized beforehand. For example, on a P type board, the thin layer of P^+-Si and the thin layer of P type Si which contained boron in the concentration 10^{19} / more than cm^3 are laminated by methods, such as epitaxial growth, and it is considered as the 1st substrate. After pasting this together to the 2nd substrate via insulating layers, such as an oxide film, the rear face of the 1st substrate is beforehand made thin by grinding and polish. Then, they are exposure and a thing which exposes a P type layer by the selective etching of a P^+ layer further, and completes SOI structure about a P^+ layer in the selective etching of a P type layer. This method is detailed to the report of Maszara (W. P.Maszara, J.Electrochem.Soc., vol.138,341 (1991)).

[0018]although selective etching is effective in uniform thin-film-izing - 10^2 and a selection ratio are not enough at most.

[0019]- Since the surface nature after etching is bad, a touch polish is needed after etching. However, as a result, while thickness decreases, thickness uniformity also deteriorates easily. Although especially polishing manages polishing quantity by time, since dispersion in polishing speed is large, control of polishing quantity is difficult. Therefore, in formation of an ultra-thin SOI layer, such as 100 nm, it becomes especially a problem.

[0020]- Since the epitaxial growth on an ion implantation and a high concentration B dope Si layer or heteroepitaxial growth is used, the crystallinity of a SOI layer is bad. The surface nature of a lamination side is also inferior to the usual Si wafer. . There is a problem of **. C. -- Harendt and et.al.. J. Elect.Mater.Vol.20,267. (1991) H.Baumgart,et.al.,Extended Abstract of ECS 1st International Symposium of Wafer Bonding,pp-733(1991),C.E. Hunt, Extended Abstract of ECS 1 st International Symposium of Wafer Bonding, pp-696 (1991). It depends for the selectivity of selective etching on the density difference and the steepness of a depth direction profile of impurities, such as boron, greatly. Therefore, if hot epitaxial growth is performed in order to raise hot bonding annealing for raising lamination intensity, and crystallinity, depth direction distribution of impurity concentration will spread and the selectivity of etching will deteriorate. That is, coexistence of improvement in lamination intensity was difficult for the crystallinity of improvement in the selection ratio of etching.

[0021]Meanwhile, these people proposed the manufacturing method of the new semiconductor member in JP,5-21338,A previously. The method indicated by the gazette concerned is a thing as follows. Namely, the member which allotted the nonvesicular single crystal semiconductor field is formed on a porosity single crystal semiconductor field, After the surface pastes together to the surface of said nonvesicular single crystal semiconductor field the surface of the member which

comprised an insulating material, it is a manufacturing method of the semiconductor member removing said porosity single crystal semiconductor field by etching.

[0022]Maibara and others which is the artificers of this invention was excellent in thickness uniformity or crystallinity, and reported lamination SOI in which batch processing is possible (T. Yonehara et.al., Appl.Phys.Lett.vol.64-2108 (1994)). Hereafter, the manufacturing method of this lamination SOI is explained using drawing 3 (a) - (c).

[0023]In this method, the porous layer 32 on Si substrate 31 is used as a material which performs selective etching. After growing the nonvesicular single crystal Si layer 33 epitaxially on the porous layer 32, it pastes together to the 2nd substrate 34 via oxidation Si layer 35 (drawing 3 (a)). Lamination of the 1st substrate is carried out by methods, such as grinding, from a rear face, and porosity Si is exposed in an entire substrate (drawing 3 (b)). Exposed porosity Si is etched with selective etching liquid, such as KOH and $HF+H_2O_2$, and is removed (drawing 3 (c)). Since the selection ratio of etching to bulk Si (nonvesicular single crystal Si) of porosity Si can be made high enough with 100,000 times at this time, The nonvesicular single crystal Si layer beforehand grown-up on porosity can be transferred on the 2nd substrate, without reducing most thickness (transfer), and a SOI substrate can be formed. Therefore, the thickness uniformity of SOI is mostly determined at the time of epitaxial growth. Since the epitaxial growth can use the CVD system usually used by a semiconductor process, as for the homogeneity, according to the report (SSDM95) of Sato and others, less than [100nm**2%] is realized. The crystallinity of the epitaxial Si layer was also good and $3.5x10^{2}/cm^{2}$ was reported.

[0024]By the conventional method, since the selectivity of etching was based on the difference and the profile of a depth direction of impurity concentration, the temperature (pasting together epitaxial growth, oxidation, etc.) of heat treatment which extends concentration distribution was greatly restrained in general with 800 ** or less. On the other hand, since etching in this method has determined the speed of etching of the difference of porosity and the structure of bulk, it is reported that restrictions of heat treatment temperature are small and heat treatment of about 1180 ** is possible. For example, heat treatment after pasting raises the adhesive strength of wafers, and decreasing the number of the openings (void) produced in a lamination interface and a size is known. ** -- by etching based on a structure difference [like], even if there is particle which adhered on porosity Si, thickness uniformity is not affected.

[0025]However, the semiconductor substrate using lamination certainly needs two wafers, most is almost vainly removed by polish, etching, etc., and one sheet of them is thrown away.

The resources of the limited earth are useless.

Therefore, in SOI by lamination, the controllable and homogeneous formation of other low cost and improvement in economical efficiency are just going to desire.

[0026]That is, while quality produced sufficient SOI substrate with sufficient reproducibility, saving resources by the reuse of a wafer, etc. and a method of realizing a cost cut were desired simultaneously.

[0027]Meanwhile, after these people pasted the substrate of two boards together previously, they

separated the stuck substrate in the porous layer, removed remains porosity from one substrate after separation, and proposed the manufacturing method of the semiconductor substrate which reuses this substrate by JP,7-302889,A.

[0028]Drawing 4 (a) - (c) is used for below, and one example of the method indicated by the gazette concerned is explained to it.

[0029]After porosity-izing the surface layer of 1st Si substrate 41 and forming the porous layer 42, the single crystal Si layer 43 is formed on it, and this single crystal Si layer and 1st Si base paste together the principal surface of 2nd another Si substrate 44 via the insulating layer 45 (drawing 4 (a)). Then, a SOI substrate is formed by dividing the wafer pasted together in the porous layer (drawing 4 (b)), and removing selectively the porous Si layer exposed to the surface by the side of the 2nd Si base (drawing 4 (c)). The 1st substrate 41 can remove and reuse the porous layer which remained. And suppose that division of the wafer pasted together can be made, for example using the following technique.

[0030]. Namely, apply uniformly still more sufficient the hauling power thru/or the pressure in a field to - perpendicular direction. - Make - wafer's end face which impresses wave energies, such as an ultrasonic wave, express a porous layer, . Etch porosity Si to some extent and insert a thing like the blade of a razor there. - After making the wafer's end face express a porous layer and infiltrating fluids, such as water, into porosity Si, The method of heating or cooling the whole lamination wafer and expanding a fluid of applying power to the 2nd (or the 1st) substrate horizontally to the - 1st (or the 2nd) board and destroying a porous Si layer by the method of ** is used.

[0031]Each of these is based on it being thought that it is weaker enough than bulk Si, although the mechanical strength of porosity Si is dependent on porosity. For example, as long as porosity is 50%, a mechanical strength may be considered to be a half of bulk. That is, when it compresses into a lamination wafer, and it pulls or shearing force is applied, a porous Si layer will be destroyed first. If porosity is made to increase, a porous layer can be destroyed by weaker power. However, since it was necessary actually on porosity Si to carry out quality epitaxial growth, porosity of the surface layer was made small, and it was desirable to make a device which enlarges porosity by the side of an inside in order to make it dissociate. For this reason, controlling the current energized at the time of anodization, and changing porosity was performed as written also to the example of JP,07-302889,A.

[0032]Although JP,8-213645,A is made to produce a fracture mechanically in a porous layer on the other hand and the method of separating an element formation layer from a base is indicated, the lamination of porosity of a porous layer is not indicated. Anyway, in order to separate a substrate bordering on a porous layer in this way, a porous layer is broken using a mechanical technique, or the current at the time of anodization is controlled, and porosity is made to change.

[0033]When applying external force to a lamination wafer, separating a substrate bordering on a porous layer and the adhesive strength of a lamination side is weak compared with the intensity of a porous Si layer, or when a weak portion exists locally, there is a possibility that two wafers may be divided in respect of lamination. Even if it is a case of the technique of not using the lamination

process, in order to dissociate well mechanically in a porous layer, the detailed control for separation is needed.

[0034]A bubble layer is made by an ion implantation to JP,5-211128,A, a crystal rearrangement and condensation of air bubbles are produced by heat treatment, and the method of stripping bordering on a bubble layer is proposed. In this method, optimization of heat treatment is further performed at the low temperature of 400-600 ** rather than is easy. In such low temperature, as mentioned above, generating of a void cannot be suppressed, and even if it carries out elevated-temperature reheating treatment of the void produced once after thin-film-izing, it does not disappear. That is, the number of voids and reduction of a size are the phenomena produced when high temperature heat treatment is carried out, where two wafers are ******(ed), and even if it carries out high temperature heat treatment after thin-film-izing, a void does not decrease only by the intensity of an adhesion part becoming strong. It is necessary to grind and carry out flattening of the surface after removing, and degradation of thickness distribution arises in this method.

[0035]As explained above, although there are some which should be made a technical problem, respectively in the method of separating a substrate bordering on a porous layer, the field of the invention of lamination SOI art is expanded, and the solution is going to just desire so that it may explain below.

[0036]The light transmittance state board represented by glass constitutes the contact sensor which is an optical photo detector, and a projected type liquid crystal image display device, and also is important. and the pixel (picture element) of a sensor or a display -- more -- much more -- densification and high-resolution-izing -- in order to become highly minute, a highly efficient driver element is needed. As a result, it is necessary to be produced using the single crystal layer which has the crystallinity outstanding also as an element provided on the light transmittance state board. If a single crystal layer is furthermore used, the peripheral circuit which drives a pixel, and the circuit for image processing can be included in the same substrate as a pixel, and miniaturization and improvement in the speed of a chip can be attained.

[0037]However, on the light transmittance state board represented by glass, generally, from the disorderly nature of the crystal structure, reflecting the disorderly nature of a substrate, the deposited thin film Si layer is amorphous, or is not good, and turns into only a polycrystalline layer, and a highly efficient device cannot be produced. it has an amorphous crystal structure of a substrate -- **** . Even if it deposits a Si layer, a good single crystal layer is not obtained.

[0038]That is, in amorphous Si or polycrystal Si, it is difficult to produce a crystal structure with many the defect, therefore the driver element which is required or had sufficient performance to be required from now on. Therefore, SOI art, such as lamination SOI which was mentioned above, is desired.

[0039]Although the substrate of a compound semiconductor is indispensable to the device manufacturing of a compound semiconductor, a compound semiconductor substrate is expensive, a mechanical strength is low, and a large area wafer has which problem with difficult production. From such a thing, it is cheap, a mechanical strength is also high, and the trial which carries out

heteroepitaxial growth of the compound semiconductor on the Si wafer which can produce a large area wafer is made.

[0040]However, although to grow epitaxially compound semiconductors, such as GaAs, on a Si substrate is tried, it is very difficult for the growth film to have bad crystallinity and to apply to a device by the difference in a grating constant or a coefficient of thermal expansion.

[0041]On the other hand, in order to ease the misfit of a lattice, to grow a compound semiconductor epitaxially on porosity Si is tried, but the stability as a substrate under production or after producing, and reliability are missing in a device by the thermal stability lowness of porosity Si, aging, etc. Then, after growing a compound semiconductor epitaxially on porosity Si, use of lamination SOI art of moving a compound semiconductor to other substrates which was mentioned above can be considered.

[0042]The purpose of this invention is a manufacturing method of the semiconductor member which has the process of pasting two bases together, and there is in providing the manufacturing method of the semiconductor member which can reuse one copy of this base as raw material of this semiconductor member.

[0043]

[Means for Solving the Problem]A process for which a manufacturing method of a semiconductor member of this invention prepares the 1st base in which a nonvesicular semiconductor layer was allotted on said porous silicon layer of a silicon substrate which has a porous silicon layer, A process of pasting said 1st base and the 2nd base together so that a multilayer-structure object in which said nonvesicular semiconductor layer is located inside may be acquired, It has a process of separating said multilayer-structure object in said porous silicon layer, and the process of removing a porous silicon layer which remained in said separated 2nd base side, by heating said multilayer-structure object.

[0044]A process for which a manufacturing method of a semiconductor member of this invention prepares the 1st base in which a nonvesicular semiconductor layer was allotted on said porous silicon layer of a silicon substrate which has a porous silicon layer, A process of pasting said 1st base and the 2nd base together so that a multilayer-structure object in which said nonvesicular semiconductor layer is located inside may be acquired, A process of separating said multilayer-structure object in said porous silicon layer by heating said multilayer-structure object, It has a process of removing a porous silicon layer which remained in said separated 2nd base side, and the process of using a base produced by removing a porous silicon layer which remained in said separated 1st base side as raw material material of said 1st base.

[0045]A process for which a manufacturing method of a semiconductor member of this invention prepares the 1st base in which a nonvesicular semiconductor layer was allotted on said porous silicon layer of a silicon substrate which has a porous silicon layer, A process of pasting said 1st base and the 2nd base together so that a multilayer-structure object in which said nonvesicular semiconductor layer is located inside may be acquired, A process of separating said multilayer-structure object in said porous silicon layer by heating said multilayer-structure object, It has a process of removing a

porous silicon layer which remained in said separated 2nd base side, and the process of using a base produced by removing a porous silicon layer which remained in said separated 1st base side as raw material material of said 2nd base.

[0046]In a method of applying the external pressure to a lamination base of the conventional multilayer structure, and separating a base by porosity Si, an interface with weak intensity, and when there is a weak field selectively, will separate from there, but. This invention can use that porosity Si is structurally vulnerable, can heat the whole multilayer-structure object pasted together, porosity Si, or its neighborhood, and can make heat stress at that time, or softening separate a base bordering on porosity Si. Therefore, lamination of a porous Si layer is not a problem, may be uniform or may make porosity come to change in layers. According to this invention, since the brittleness of porosity Si can be used and internal pressure can be applied to a porous Si layer with heat stress, thereby, a base can be divided with sufficient control in a porous Si layer.

[0047]Since production of the conventional lamination base uses how grinding and etching remove the 1st base (Si base) from one side one by one, it is impossible to use both sides of the 1st base effectively and to paste together to a supporting board, but. Since same maintenance of the 1st base (Si base) is carried out except the surface layer according to this invention, By making both both sides of the 1st base into the principal surface, and pasting a supporting board together to the field, respectively, two lamination boards can also be simultaneously produced from the 1st base of one sheet, and productivity can be improved. Of course, the 1st separated base can be reused.

[0048]And since this invention can be collectively divided into a large area via a porous layer when it removes the 1st base, A process is shortened and it excels in economical efficiency, and over a large area, a yield can be good for the 2nd base and nonvesicular thin films, such as a uniformly flat Si single crystal layer which has the extremely outstanding crystallinity, or a compound semiconductor single crystal layer, can be transferred. Namely, the homogeneity of a Si single crystal layer of thickness is good, and, moreover, it can acquire SOI structure formed on an insulating layer with a sufficient yield.

[0049]In this invention, when using laser for heating, without heating the whole lamination base, only a certain specific layer is made to absorb energy, and it can heat. therefore, partial heating can be performed by using laser of wavelength seen and absorbed to that of a porous Si layer or a layer near the porosity Si.

[0050]In this invention, a porous Si layer can be heated by energizing current in a wafer surface a porous Si layer or near the porosity Si.

[0051]According to this invention, the 1st base (Si base) after separating a porous substrate can be reused. It can carry out a reuse any number of times until it becomes impossible in intensity to use this 1st base (Si base).

[0052]According to this invention, in order to remove the 1st base since two bases can be put in block to a large area and it can separate into it bordering on a porous layer, and to expose a porous Si layer, grinding which was being performed conventionally, polish, and an etching process can be skipped, and a process can be shortened. And by carrying out the ion implantation of at least one sort

of elements among rare gas, hydrogen, and nitrogen, beforehand, so that it may have a projection range in this porous layer, since a position to separate can be specified to a place of the limited depth in a porous Si layer, thickness of an elaborate porous layer which a 2nd base side boils becomes uniform, and it becomes possible [an etching reagent of selectivity which is not so good] to remove a porous layer uniformly.

[0053]According to this invention, it excels in economical efficiency and uniformly flat nonvesicular semiconductor layers (a Si layer or a compound layer) which have the extremely outstanding crystallinity can be formed on the 2nd base (a semiconductor, an insulator, etc.) over a large area.

[0054]This invention can provide a manufacturing method of a semiconductor member which stood high in a field of productivity, homogeneity, controllability, and cost, when crystallinity obtains nonvesicular semiconductor layers (Si or a compound semiconductor single crystal layer) outstanding just like the single crystal wafer on a transparent substrate (light transmittance state board).

[0055]According to this invention, a semiconductor member constituted by allotting a uniformly flat single crystal semiconductor layer which has the extremely outstanding crystallinity can be provided over a large area by performing selective etching in which a selection ratio is preeminently excellent.

[0056]According to this invention, when producing large scale integration circuit of SOI structure, expensive SOS and a manufacturing method of alternative ********** of SIMOX can be provided.

[0057]

[Embodiment of the Invention]Although the suitable example of an embodiment of this invention is described hereafter, this invention is not limited to these examples of an embodiment, and the purpose of this invention should just be attained.

[Formation of porous silicon] Porosity Si was discovered by Uhlir etc. in the research process of electrolytic polishing of a semiconductor in 1956 (A. Uhlir, Bell Syst.Tech.J., vol.35,333 (1956)). Porosity Si can be formed by carrying out anodization (Anodization) of the Si substrate in an HF solution. Unagami studied the lytic reaction of Si in anodization, an electron hole is required for the anodic reaction of Si in an HF solution, and the reaction has reported that it is as follows (T. Unagami, J.Electrochem.Soc., vol.127,476 (1980)).

[0058]$Si+2HF+(2-n)\ e^{+} \rightarrow SiF_2+2H^{+}+ne^{-}\ SiF_2+2HF \rightarrow SiF_4+H_2SiF_4+2HF \rightarrow H_2SiF_6$ -- or, $Si+4HF+(4-lambda)\ e^{+} \rightarrow SiF_4+4H^{+}+lambdae^{-}\ SiF_4+2HF \rightarrow H_2SiF_6$ -- here, e^{+} and e^{-} express the electron hole and the electron, respectively. n and lambda are the number of electron holes required in order that one atom of Si may dissolve, respectively, and when n> 2 or the conditions which become lambda>4 are fulfilled, they suppose that porosity Si is formed.

[0059]Although it will be said that P type Si in which an electron hole exists considering the above thing is porosity-ized, and N type Si is not porosity-ized,-izing also of the N type Si can be carried out [porosity] by changing conditions.

[0060]In this invention, porosity Si which has single crystal nature can be formed by carrying out anodization (Anodization) of the single crystal Si substrate for example, in an HF solution. The porous

layer is having structure like sponge where the hole of the about [10^{-1}-10nm] diameter was located in a line at the interval which is about 10^{-1}-10nm. The density can be changed to the range of 2.1 - 0.6 g/cm^3 by changing HF solution concentration to 50 to 20%, or changing current density compared with density 2.33 g/cm^3 of single crystal Si. That is, it is possible to change Porosity. Thus, in spite of making density of porosity Si to below half compared with single crystal Si, single crystal nature is maintained and it is also possible to grow a single crystal Si layer epitaxially to the upper part of a porous layer.

[0061]Since a lot of [a porous layer] openings to the inside are formed, density decreases below in half. As a result, since surface area increases by leaps and bounds compared with volume, the chemical etching speed is remarkably accelerated compared with the etch rate of the usual single crystal layer.

[0062]Although the mechanical strength of porosity Si changes with porosit(ies), it is thought that it is weaker than bulk Si. For example, as long as porosity is 50%, a mechanical strength may be considered to be a half of bulk. That is, when it compresses into a lamination wafer, and it pulls or shearing force is applied, a porous Si layer will be destroyed first. If porosity is made to increase, a porous layer can be destroyed by weaker power.

[0063]In bulk Si, helium and hydrogen. . It is reported that a minute cave (micro-cavity) several nanometers - tens of nm in diameter is formed in the field poured in when the ion implantation was carried out and heat treatment was added by -$10^{16\text{-}17}$ / cm^3 thing density. (For example, A.Van Veen,C.C.Griffioen,and J.H.Evans,Mat.Res.Soc.Symp.Proc.107(1988,Material Res.Soc.Pittsburgh,Pennsylvania)p.449.) .Using these microporosity group as a gettering site of a metal impurity these days is studied.

[0064]V. After Raineri and S.U.Campisano formed the cavernous group which poured in helium ions, heat-treated and was formed into bulk Si, they formed the slot in the substrate, exposed the side of the cavernous group, and performed oxidation treatment. As a result, the cavernous group oxidized selectively, was embedded and formed the oxidation Si layer. That is, it reported that SOI structure could be formed (V. Raineri, and S.U.Campisano, Appl.Phys.Lett.66(1995)p.3654). However, by their method, embed with a surface Si layer, and the thickness of the oxidation Si layer is limited to the point of reconciling both relaxation of the stress introduced by formation of a cavernous group, and the cubical expansion at the time of oxidation, and also needs formation of a slot because of selective oxidation, SOI structure was not able to be formed in the entire substrate.

[0065][Nonvesicular semiconductor layer] In this invention, as a nonvesicular semiconductor layer, Conveniently, compound semiconductors, such as InP, GaAsP, GaAs, GaAlAs besides single crystal Si, polycrystal Si, and amorphous Si, InAs, AlGaSb, InGaAs, ZnS, CdSe, CdTe, and SiGe, etc. can be used. And a nonvesicular semiconductor layer may already make semiconductor devices, such as FET (Field Effect Transistor).

[0066]The [1st base] In this invention, the 1st base refers to what was matched with the nonvesicular semiconductor layer on the porous layer of the silicon substrate which has a porous silicon layer.

Therefore, the 1st base also includes that by which insulator layers, such as a further different layer, for example, SiN, and a SiO_2 film, etc. were formed on the nonvesicular semiconductor layer.

[0067]As an example, the 1st base can be constituted by forming a porous silicon layer selectively into the silicon substrate which formed the above-mentioned nonvesicular semiconductor layer on the porous silicon layer formed into the silicon substrate or in which the nonvesicular semiconductor layer was provided.

[0068]In order to form a nonvesicular semiconductor layer on a porous silicon layer, A sputtering technique (a bias sputtering technique is included), molecular beam epitaxy, a liquid phase epitaxy method, etc. besides CVD methods, such as the decompression CVD, plasma CVD, the light CVD, and MOCVD (Metal-Organic CVD), are employable.

[0069]The [2nd base] as the 2nd base by which a nonvesicular semiconductor layer is transferred (transfer), For example, insulating substrates, such as a semiconductor substrate like a single crystal silicon substrate, a thing which provided insulator layers, such as an oxide film (an oxidizing film is included) and a nitride, in the semiconductor substrate surface, a quartz substrate (Silica glass) and a light transmittance state board like a glass substrate or a metal substrate, and alumina, etc. are raised. Such 2nd base is suitably chosen according to the use of a semiconductor member.

[0070][Lamination] In this invention, said 1st base and the 2nd base are pasted together so that the multilayer-structure object in which a nonvesicular semiconductor layer is located inside may be acquired. In this invention, a multilayer-structure object includes not only that by which the nonvesicular semiconductor layer of the 1st base was directly stuck on the 2nd base but the multilayer-structure object in which insulating layers etc. which were formed on the nonvesicular semiconductor layer, such as SiN and SiO_2, stick on the 2nd base, are together put, and are constituted.

[0071]By what the lamination side of the 1st base and the 2nd base is made flat for, it can paste together by sticking both at a room temperature. In addition, since lamination intensity is increased, anode joining, application of pressure, heat treatment, etc. can also be performed.

[0072][Heating of a multilayer-structure object] In this invention, the 1st base that has a porous silicon layer and a nonvesicular semiconductor layer The 2nd above-mentioned base, After acquiring lamination (it is located inside like [a nonvesicular semiconductor layer]) ** and a multilayer-structure object, in order to transfer a nonvesicular semiconductor layer to the 2nd base side, a multilayer-structure object is separated in a porous silicon layer. Although carried out by heating a multilayer-structure object, this separation is included with this heating, also when heating selectively the particular part which constitutes a multilayer-structure object besides heating the whole multilayer-structure object, for example, a porous silicon layer. The method of heating a multilayer-structure object at about 600-1200 **, and the method of not heating the whole multilayer-structure object, but making only a certain specific layer absorb energy, and heating a specific layer by laser radiation, are also employable, using a furnace (for example, heat treating furnace) as a concrete heating method. In the case of the latter, partial heating can be performed by using the laser of the wavelength

absorbed by only a porous Si layer or the layer near the porosity Si.
[0073]There is also a method of heating a porous Si layer as an example of partial heating by sending current in the wafer surface a porous Si layer or near the porosity Si.
[0074][Removal of a porous layer] after separating the multilayer-structure object acquired by pasting the 1st base and 2nd base together in a porous Si layer, the porous Si layer which remains to the separated base, It is selectively removable using that the mechanical strength of this porous Si layer is low, and surface area being dramatically large. Methods using an etching reagent besides the mechanical method using grinding and polish as an alternative removing method, such as chemical etching and ion etching (for example, reactive ion etching), are employable.
[0075]When carrying out selective etching of the porous Si layer using an etching reagent, as an etching reagent, The mixed liquor which added alcohol 49% not only to the mixed liquor of fluoric acid and 30% hydrogen peroxide solution but to fluoric acid and fluoric acid, Mixed liquor, buffered fluoric acid which added alcohol and hydrogen peroxide solution to fluoric acid, A thing like the mixed liquor which added alcohol to buffered fluoric acid, the mixed liquor which added hydrogen peroxide solution to buffered fluoric acid, the mixed liquor which added alcohol and hydrogen peroxide solution to buffered fluoric acid, or the mixed liquor of fluoric acid, nitric acid, and acetic acid is employable. After carrying out selection removal of the porous layer, the surface smoothness of a nonvesicular semiconductor layer can be increased by heat-treating the semiconductor member produced by a nonvesicular semiconductor layer being transferred under the atmosphere containing hydrogen.
[0076]Hereafter, an embodiment of the invention is described using a drawing.
[0077][Example 1 of an embodiment] As shown in drawing 1 (a), 1st Si single crystal substrate 11 is prepared first, the nonvesicular thin film 13 of at least one layer is formed in the outermost superficial layer of the principal surface, and the porous Si layer 12 is formed directly under it. Manufacturing methods of the nonvesicular thin film 13 and the porous Si layer 12 include the following method.
[0078]a) How to form the nonvesicular thin film 13 on this porous Si layer after forming the porous Si layer 12 by anodization.
[0079]b) How to carry out the ion implantation of a kind of element at least among rare gas, hydrogen, and nitrogen, and carry out the simultaneously form of the porous Si layer 12 and the nonvesicular thin film 13.
[0080]c) How to carry out the ion implantation of a kind of element to a at least among rare gas, hydrogen, and nitrogen further, and form the field where porosit(ies) differ.
or [********] -- from -- it is chosen. The nonvesicular thin film 13 is arbitrarily chosen out of single crystal Si, polycrystal Si, amorphous Si or a metal membrane, a compound semiconductor thin film, a superconducting thin film, etc. Or element structures, such as MOSFET, may be formed. The direction which formed SiO_2 in the outermost superficial layer may mean that the interface state density of a lamination interface can be separated from an active layer. When a pouring layer is observed with a transmission electron microscope etc., it turns out that microporosity is formed innumerably. As for the ion to pour in, a charge state in particular is not limited. Accelerating energy is set up so that a projection range may come to the depth to pour in. Although the size of the

microporosity formed and density change according to an injection rate, the injection rates of more than 1x10 ^{14}/cm^2 are 1x10 ^{15}/cm^2 more preferably in general. It does not matter by a channeling ion implantation to set up a projection range deeply, either. After pouring, it heat-treats if needed. As shown in drawing 1 (a), the surface of the 2nd substrate 14 and the 1st substrate is stuck at a room temperature. Then, lamination may be strengthened with heat treatments or such combination anode joining, application of pressure, or if needed.

[0081]When deposition formation of the single crystal Si is carried out, it is preferred to paste together, after forming oxidation Si in the surface of single crystal Si by methods, such as thermal oxidation. Although it can choose from light transmittance state boards, such as Si, a thing in which the oxidation Si film was formed on the Si substrate, and quartz, sapphire, etc., the 2nd substrate is not limited to this, and if the field with which lamination is presented is flat enough and there is, it will not be cared about. Although drawing 1 (a) has shown signs that the 2nd substrate and 1st substrate were pasted together via the insulating layer 15, when the nonvesicular thin film 13 is not Si, or when the 2nd substrate is not Si, it may not have the insulating layer 15. It is also possible to paste together by a three-sheet pile on both sides of insulating sheet metal on the occasion of lamination.

[0082]Even if it is a case where are things other than this and a nonvesicular thin film is constituted when it constitutes from single crystal silicon which grew the nonvesicular thin film epitaxially or, When using heat treatment at heat treatment at the time of epitaxial growth, and the process after this, the rearrangement of the hole inside a porous silicon layer arises with heat, a hole is closed, and there is a possibility that the etching properties at the time of carrying out etching removal of the porous layer may be spoiled. Then, it is possible to heat-treat beforehand at the temperature of 200 ** - about 700 **, to, form a thin oxide film (the single crystal nature as a porous layer is maintained) in the side attachment wall of a hole for example, to prevent a rearrangement, and to stabilize the structure of a porous layer.

[0083]The following process is also employable in order to form an epitaxial silicone film with very few defects.

[0084]Although the porous silicon layer is maintaining the structure as a single crystal, it originates in the hole of a large number which exist on the surface of a porous silicon layer, and a defect may go into an epitaxial silicone film. Then, the technique of blockading the outermost surface of a porous silicon layer where an epitaxial silicone film contacts with single crystal silicon can be considered.

[0085]One of the method of this has heat treatment in the atmosphere containing hydrogen. The migration of the silicon atom which constitutes the surface of porous silicon depending on this hydrogen heat treatment arises, and the outermost surface of the hole of a porous silicon layer is blockaded. The ranges of 500 ** - 1300 ** of temperature of heat treatment in this case are 900 ** - 1300 ** preferably.

[0086]A silicone film can be formed at a very slow speed by passing a little material gas containing a silicon atom in a film forming chamber apart from this technique, and the outermost surface of the hole of a porous silicon layer can also be made to blockade.

[0087]When performing blockade of a hole, and formation of an epitaxial silicone film after forming a

thin oxide film in the side attachment wall of an above-mentioned hole and making a hole blockade, it is desirable for the single crystal to be exposed to the outermost surface of a porous silicon layer. The outermost surface of the porous silicon layer which formed the thin oxide film in the side attachment wall of a hole can be attached to acid, such as HF, and exposure of this single crystal can be performed by removing the thin oxide film formed in the outermost surface.

[0088]Next, it pastes together, and the whole base (multilayer-structure object), porosity Si, or its neighborhood is heated, it pastes together bordering on a porous Si layer by the heat stress at that time, or softening, and a base is made to separate (drawing 1 (b)). The whole base may be heated with a heat treating furnace. Or partial heating is performed by using the laser of the wavelength absorbed only in a porous Si layer or the layer near the porosity Si. A porous Si layer can also be heated by energizing current in a wafer surface a porous Si layer or near the porosity Si.

[0089]Porosity Si12 is removed selectively. Fluoric acid which is an etching reagent of usual Si, or selective etching liquid of porosity Si when a nonvesicular thin film is single crystal Si, To fluoric acid, or alcohol and mixed liquor of hydrogen peroxide solution which added either at least, Or at least one kind of the mixed liquor of alcohol and hydrogen peroxide solution which added either at least is used for buffered fluoric acid or buffered fluoric acid, The film which carried out unelectrolyzed wet chemical etching only of porosity Si12, and was beforehand formed on the porosity of the 1st substrate on the 2nd substrate is made to remain. As it explained [above-mentioned] in full detail, it is possible for the etching reagent of usual Si to also etch only porosity Si selectively with the huge surface area of porosity Si. Or porosity Si12 is removed by selection polish by making the nonvesicular thin film layer 13 into a polishing stopper.

[0090]When the compound semiconductor layer is formed on porosity, chemical etching only of porosity Si12 is carried out using an etching reagent with a quick etch rate of Si to a compound semiconductor, and on the 2nd substrate 14, the thin-film-ized single crystal compound semiconductor layer 13 is made to remain, and it forms. Or porosity Si12 is removed by selection polish by making the single crystal compound semiconductor layer 13 into a polishing stopper.

[0091]The semiconductor member obtained by this invention is shown in drawing 1 (c). On the 2nd substrate 14, lamination of the nonvesicular thin film 13, for example, the monocrystal Si thin film, is carried out evenly and uniformly, and it is formed throughout a wafer at a large area. If an insulating substrate is used as the 2nd substrate 14, the semiconductor substrate obtained in this way can be conveniently used, even if it sees from the point of electronic device production by which insulated separation was carried out.

[0092]1st Si single crystal substrate 11 removes remains porosity Si, and when ruined so that it cannot permit surface evenness, after it performs surface flattening, it can use it again as 1st Si single crystal substrate 11 or the 2nd following base 14.

[0093][Example 2 of an embodiment] As shown in drawing 2, this example of an embodiment forms the porous Si layer 22 and the nonvesicular thin film 23 in both sides of 1st Si single crystal substrate 21 used as the 1st base, pastes the 2nd base 24 and 25 together to each field via the insulating layer 26, and produces two semiconductor substrates simultaneously. Each manufacturing process is the

same as that of the process shown in the above-mentioned example 1 of an embodiment.
[0094]1st Si single crystal substrate 21 removes remains porosity Si, and when ruined so that it cannot permit surface evenness, after it performs surface flattening, it can use it again as 1st Si single crystal substrate 21 or the 2nd following base 24 (or 25).
[0095]The material of the supporting boards 24 and 25, the thickness, etc. may not be the same. The nonvesicular thin film 23 does not have to make both sides the same material, thickness, etc.
[0096]
[Example]Hereafter, an example is given concretely and this invention is explained.
[0097](Example 1) Into the HF solution, anodization was performed to the surface layer of the 1st single crystal Si substrate. The anodization conditions were as follows.
[0098]

Current density: 7 ($mA\text{-}cm^{-2}$)
Anodization solution: $HF:H_2O:C_2H_5OH$= 1:1:1:00 Between: 11 (minute)

thickness [of porosity Si]: -- 12 (micrometer)
This substrate was oxidized at 400 ** among oxygen environment for 1 hour. The wall of the hole of porosity Si was covered with this oxidation with the oxidizing film. 0.15 micrometer grew single crystal Si epitaxially by the CVD (Chemical Vapor Deposition) method on porosity Si. The growing condition is as follows.
[0099]
Source gas: SiH_2Cl_2/H_2 gas mass flow : 0.5 / 180 l/min gas pressure : 80Torr ** Degree : 950 ** growth rate : To a 0.3 micrometer/min pan. A 100-nm SiO_2 layer was formed in this epitaxial Si layer surface by thermal oxidation.
[0100]This SiO_2 layer surface and the surface of the Si substrate (the 2nd substrate) in which the 500-nm SiO_2 layer prepared apart from this was formed on the surface were piled up, and were contacted. Thereby, the multilayer-structure object was formed.
[0101]After removing the rear-face oxide film of the 1st substrate, the entire wafer surface was irradiated with CO_2 laser of the about [500-1000W] output from the 1st substrate side. It was absorbed by the 500-nm SiO_2 layer of the lamination interface, the temperature of the epitaxial layer of the neighborhood and the porous Si layer rose rapidly, and the rapid heat stress in a lower porous Si layer separated CO_2 laser in the lower porous Si layer. Continuation or a pulse is also available for laser.
[0102]Then, selective etching was carried out, stirring the porous Si layer which remained in the 2nd substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single crystal Si remained without being etched, as a material of an etch stop, selective etching of the porosity Si was carried out, and single crystal Si was removed thoroughly.
[0103]The etch rate to this etching reagent of a nonvesicular Si single crystal is very low, the selection

ratio with the etch rate of a porous layer amounts to the fifth power or more of 10, and the etching quantity (about tens of A) in a nonvesicular layer is thickness reduction which can be disregarded practically.

[0104]That is, the single crystal Si layer which had a thickness of 0.1 micrometer on the Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 101nm**3nm.

[0105]Furthermore, it heat-treated at 1100 ** in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of a 50-micrometer angle was equivalent to the Si wafer usually marketed at about 0.2 nm.

[0106]As a result of the section observation by a transmission electron microscope, a new crystal defect was not introduced into a Si layer, but it was checked that good crystallinity is maintained.

[0107]The same result was obtained even if it did not form an oxide film in the epitaxial Si layer surface.

[0108]Selective etching was carried out also stirring after that porosity Si which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single crystal Si remained without being etched, and as a material of an etch stop, selective etching of the porosity Si was carried out, it was removed thoroughly, and was able to supply single crystal Si to the oxide film formation process as an anodization process or the 2nd substrate as the 1st substrate again.

[0109](Example 2) Into the HF solution, anodization was performed to the surface layer of the 1st single crystal Si substrate. The anodization conditions were as follows.

[0110]

Current density: 7 ($mA\text{-}cm^{-2}$)

Anodization solution: $HF:H_2O:C_2H_5OH$= 1:1:1:00 Between: 11 (minute)

thickness [of porosity Si]: -- 12 (micrometer)

This substrate was oxidized at 400 ** among oxygen environment for 1 hour. The wall of the hole of porosity Si was covered with this oxidation with the oxidizing film. 0.15 micrometer grew P^+ single crystal Si epitaxially by the CVD (Chemical Vapor Deposition) method on porosity Si. The growing condition is as follows. B_2H_6 was introduced as impurity gas.

[0111]

Source gas: SiH_2Cl_2/H_2 gas mass flow : 0.5 / 180 l/min gas pressure : 80Torr ** Degree : 950 ** growth rate : To a 0.3 micrometer/min pan. A 100-nm SiO_2 layer was formed in this epitaxial Si layer surface by thermal oxidation.

[0112]This SiO_2 layer surface and the surface of the Si substrate (the 2nd substrate) in which the 500-nm SiO_2 layer prepared independently was formed were piled up, and were contacted.

[0113]About [10-100A] current was sent only through the high concentration P^+ single crystal Si

layer of the 1st substrate (the impurity concentration of a high concentration P^+ single crystal Si layer should just be the concentration which can carry out [low resistance]-izing to such an extent that it can send current.). Current removes SiO_2, makes a wafer end express a high concentration P^+ single crystal Si layer, and by + electrode and - electrode which only a wafer's end face touches, as it puts a wafer, it pours it. As a result, into the lower porous Si layer, rapid heat stress was added and it dissociated in the lower porous Si layer. Continuation or a pulse is also available for current.

[0114]Then, selective etching was carried out, stirring the porous Si layer which remained in the 2nd substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single crystal Si remained without being etched, as a material of an etch stop, selective etching of the porosity Si was carried out, and single crystal Si was removed thoroughly.

[0115]Thereby, the single crystal Si layer which had a thickness of 0.1 micrometer on the Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 101nm**3nm.

[0116]Furthermore, it heat-treated at 1100 ** in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of a 50-micrometer angle was equivalent to the Si wafer usually marketed at about 0.2 nm.

[0117]As a result of the section observation by a transmission electron microscope, a new crystal defect was not introduced into a Si layer, but it was checked that good crystallinity is maintained.

[0118]The same result was obtained even if it did not form an oxide film in the epitaxial Si layer surface.

[0119]Selective etching was carried out also stirring after that porosity Si which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single crystal Si remained without being etched, and as a material of an etch stop, selective etching of the porosity Si was carried out, it was removed thoroughly, and was able to supply single crystal Si to the oxide film formation process as an anodization process or the 2nd substrate as the 1st substrate again.

[0120](Example 3) Into the HF solution, anodization was performed to the surface layer of the 1st single crystal Si substrate. The anodization conditions were as follows.

[0121]

Current density: 7 ($mA\text{-}cm^{-2}$)

Anodization solution: $HF:H_2O:C_2H_5OH$= 1:1:1:00 Between: 11 (minute)

thickness [of porosity Si]: -- 12 (micrometer)

This substrate was oxidized at 400 ** among oxygen environment for 1 hour. The wall of the hole of porosity Si was covered with this oxidation with the oxidizing film. 0.15 micrometer grew single crystal Si epitaxially by the CVD (Chemical Vapor Deposition) method on porosity Si. The growing condition is as follows.

[0122]

Source gas: SiH_2Cl_2/H_2 gas mass flow : 0.5 / 180 l/min gas pressure : 80Torr ** Degree : 950 **

growth rate : To a 0.3 micrometer/min pan. A 100-nm SiO_2 layer was formed in this epitaxial Si layer surface by thermal oxidation.

[0123]pile up after putting the surface of the Si substrate (the 2nd substrate) in which this SiO_2 layer surface and the 500-nm SiO_2 layer prepared independently were formed to nitrogen plasma, respectively (lamination intensity is improved -- it should make) -- it was made to contact and annealed 400 ** - 10 h.

[0124]After removing the rear-face oxide film of the 1st substrate, the entire wafer surface was irradiated with CO_2 laser of the about [500-1000W] output from the 1st substrate side. It was absorbed by the 500-nm SiO_2 layer of the lamination interface, the temperature of the epitaxial layer of the neighborhood and the porous Si layer rose rapidly, and the rapid heat stress in a lower porous Si layer separated CO_2 laser in the lower porous Si layer. Continuation or a pulse is also available for laser.

[0125]Then, selective etching of the porous Si layer which remained in the 2nd substrate side was carried out with the etching reagent of a $HF/HNO_3/CH_3COOH$ system. Selective etching of the porosity Si was carried out, and it was removed thoroughly. Most single crystal Si remained without being etched, as a material of an etch stop, selective etching of the porosity Si was carried out, and single crystal Si was removed thoroughly.

[0126]The etch rate to this etching reagent of a nonvesicular Si single crystal is very low, and the etching quantity in a nonvesicular layer is thickness reduction which can be disregarded practically.

[0127]Thereby, the single crystal Si layer which had a thickness of 0.1 micrometer on the Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 101nm**3nm.

[0128]Furthermore, it heat-treated at 1100 ** in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of a 50-micrometer angle was equivalent to the Si wafer usually marketed at about 0.2 nm.

[0129]As a result of the section observation by a transmission electron microscope, a new crystal defect was not introduced into a Si layer, but it was checked that good crystallinity is maintained.

[0130]The same result was obtained even if it did not form an oxide film in the epitaxial Si layer surface.

[0131]Selective etching also of the porosity Si which remained in the 1st substrate side was carried out with the etching reagent of a $HF/HNO_3/CH_3COOH$ system after that. Single crystal Si remained without being etched, and as a material of an etch stop, selective etching of the porosity Si was carried out, it was removed thoroughly, and was able to supply single crystal Si to the oxide film formation process as an anodization process or the 2nd substrate as the 1st substrate again.

[0132](Example 4) Into the HF solution, anodization was performed to the surface layer of the 1st single crystal Si substrate. The anodization conditions were as follows.

[0133]

Current density: 7 (mA-cm^{-2})
Anodization solution: HF:H_2O:C_2H_5OH= 1:1:1:00 Between: 11 (minute)
Thickness of porosity Si: 12 (micrometer)
This substrate was oxidized at 400 ** among oxygen environment for 1 hour. The wall of the hole of porosity Si was covered with this oxidation with the oxidizing film. 0.15 micrometer grew P^+ single crystal Si epitaxially by the CVD (Chemical Vapor Deposition) method on porosity Si. The growing condition is as follows. B_2H_6 was introduced as impurity gas.

[0134]
Source gas: SiH_2Cl_2/H_2 gas mass flow : 0.5 / 180 l/min gas pressure : 80Torr ** Degree : 950 ** growth rate : To a 0.3 micrometer/min pan. A 100-nm SiO_2 layer was formed in this epitaxial Si layer surface by thermal oxidation.
[0135]This SiO_2 layer surface and the surface of the Si substrate (the 2nd substrate) in which the 500-nm SiO_2 layer prepared independently was formed were piled up, and were contacted.

[0136]About [10-100A] current was sent only through the high concentration P^+ single crystal Si layer of the 1st substrate (the impurity concentration of a high concentration P^+ single crystal Si layer should just be the concentration which can carry out [low resistance]-izing to such an extent that it can send current.). Current removes SiO_2, makes a wafer end express a high concentration P^+ single crystal Si layer, and by + electrode and - electrode which only a wafer's end face touches, as it puts a wafer, it pours it. As a result, into the lower porous Si layer, rapid heat stress was added and it dissociated in the lower porous Si layer. Continuation or a pulse is also available for current.
[0137]Then, selection polish of the porous Si layer which remained in the 2nd substrate side was carried out. Single crystal Si remained without being ground, as a material of a polish stop of single crystal Si, selection polish was carried out and porosity Si was removed thoroughly.
[0138]The polishing speed of a nonvesicular Si single crystal is very low, and polishing quantity (about tens of A) is thickness reduction which can be disregarded practically.
[0139]In this way, the single crystal Si layer which had a thickness of 0.1 micrometer on the Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 101nm**3nm.
[0140]Furthermore, it heat-treated at 1100 ** in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of a 50-micrometer angle was equivalent to the Si wafer usually marketed at about 0.2 nm.
[0141]As a result of the section observation by a transmission electron microscope, a new crystal defect was not introduced into a Si layer, but it was checked that good crystallinity is maintained.
[0142]The same result was obtained even if it did not form an oxide film in the epitaxial Si layer surface.
[0143]Porosity Si which remained in the 1st substrate side also carries out selection polish after that.

Single crystal Si remained without being ground, and as a material of a polish stop of single crystal Si, selection polish was carried out, and porosity Si was removed thoroughly, and was able to be again supplied to the oxide film formation process as an anodization process or the 2nd substrate as the 1st substrate.

[0144](Example 5) Into the HF solution, anodization was performed to the surface layer of the 1st single crystal Si substrate.

[0145]The anodization conditions were as follows.

[0146]

Current density: 7 ($mA\text{-}cm^{-2}$)

Anodization solution: $HF:H_2O:C_2H_5OH$= 1:1:1:00 Between: 11 (minute)

thickness [of porosity Si]: -- 12 (micrometer)

This substrate was oxidized at 400 ** among oxygen environment for 1 hour. The wall of the hole of porosity Si was covered with this oxidation with the oxidizing film. 0.15 micrometer grew P^+ single crystal Si epitaxially by the CVD (Chemical Vapor Deposition) method on porosity Si. The growing condition is as follows. B_2H_6 was introduced as impurity gas.

[0147]

Source gas: SiH_2Cl_2/H_2 gas mass flow : 0.5 / 180 l/min gas pressure : 80Torr ** Degree : 950 ** growth rate : To a 0.3 micrometer/min pan. A 100-nm SiO_2 layer was formed in this epitaxial Si layer surface by thermal oxidation.

[0148]pile up after putting this SiO_2 layer surface and the surface of the quartz substrate (the 2nd substrate) prepared independently to nitrogen plasma, respectively -- it was made to contact and annealed 200 ** - 10 h.

[0149]About [10-100A] current was sent only through the high concentration P^+ single crystal Si layer of the 1st substrate (the impurity concentration of a high concentration P^+ single crystal Si layer should just be the concentration which can carry out [low resistance]-izing to such an extent that it can send current.). Current removes SiO_2, makes a wafer end express a high concentration P^+ single crystal Si layer, and by + electrode and - electrode which only a wafer's end face touches, as it puts a wafer, it pours it. As a result, into the lower porous Si layer, rapid heat stress was added and it dissociated in the lower porous Si layer. Continuation or a pulse is also available for current.

[0150]Then, selective etching was carried out, stirring the porous Si layer which remained in the 2nd substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single crystal Si remained without being etched, as a material of an etch stop, selective etching of the porosity Si was carried out, and single crystal Si was removed thoroughly.

[0151]That is, the single crystal Si layer which had a thickness of 0.1 micrometer on the Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 101nm**3nm.

[0152]Furthermore, it heat-treated at 1100 ** in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of a 50-micrometer angle was equivalent to the Si wafer usually marketed at about 0.2 nm.
[0153]As a result of the section observation by a transmission electron microscope, a new crystal defect was not introduced into a Si layer, but it was checked that good crystallinity is maintained.
[0154]The same result was obtained even if it did not form an oxide film in the epitaxial Si layer surface.
[0155]Selective etching was carried out also stirring after that porosity Si which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single crystal Si remained without being etched, and as a material of an etch stop, selective etching of the porosity Si was carried out, it was removed thoroughly, and was able to supply single crystal Si to the anodization process as the 1st substrate again.
[0156](Example 6) Into the HF solution, anodization was performed to the surface layer of the 1st single crystal Si substrate.
[0157]The anodization conditions were as follows.
[0158]

Current density: 7 (mA-cm^{-2})
Anodization solution: HF:H_2O:C_2H_5OH= 1:1:1:00 Between: 11 (minute)

Thickness of porosity Si: 12 (micrometer)
This substrate was oxidized at 400 ** among oxygen environment for 1 hour. The wall of the hole of porosity Si was covered with this oxidation with the oxidizing film. 1 micrometer grew the single crystal GaAs epitaxially by the MOCVD (Metal Organic Chemical Vapor Deposition) method on porosity Si. The growing condition is as follows.
[0159]
Source gas: TMG/AsH_3/H_2 gas pressure : 80Torr ** Degree : The 700 ** this GaAs layer surface and the surface of the Si substrate (the 2nd substrate) prepared independently were piled up, and were contacted.
[0160]After removing the rear-face oxide film of the 1st substrate, the entire wafer surface was irradiated with CO_2 laser of the about [500-1000W] output from the 1st substrate side. It was absorbed by the GaAs layer, the temperature of the porous Si layer of the neighborhood rose rapidly, and the rapid heat stress in a lower porous Si layer separated CO_2 laser in the lower porous Si layer. Continuation or a pulse is also available for laser.
[0161]Then, the porous Si layer which remained in the 2nd substrate side was etched with 110 ** of ethylenediamine + pyrocatechol + water (ratio of 17 ml : 3g : 8 ml). The single crystal GaAs remained without being etched, as a material of an etch stop, selective etching of porosity Si and the porosity Si which oxidized was carried out, and the single crystal GaAs was removed thoroughly.
[0162]The etch rate to this etching reagent of a nonvesicular GaAs single crystal is very low, and the etching quantity (about tens of A) in a nonvesicular layer is thickness reduction which can be

disregarded practically.

[0163]In this way, the single crystal GaAs layer which had a thickness of 1 micrometer on Si has been formed. When 100 points were measured for the thickness of the formed single crystal GaAs layer about the whole surface within a field, the homogeneity of thickness was 1micrometer**29.8nm.

[0164]As a result of the section observation by a transmission electron microscope, a new crystal defect was not introduced into a GaAs layer, but it was checked that good crystallinity is maintained.

[0165]By using a Si substrate with an oxide film as a supporting board, GaAs on an insulator layer has been produced similarly.

[0166]Selective etching is carried out also stirring after that porosity Si which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single crystal Si remained without being etched, as a material of an etch stop, selective etching was able to be carried out, it was able to be removed thoroughly, single crystal Si was able to be again pasted together as an anodization process or the 2nd substrate as the 1st substrate, and porosity Si was able to supply it to the process.

[0167](Example 7) Into the HF solution, anodization was performed to the surface layer of the 1st single crystal Si substrate.

[0168]The anodization conditions were as follows.

[0169]

Current density: 7 ($mA\text{-}cm^{-2}$)

Anodization solution: $HF:H_2O:C_2H_5OH$= 1:1:1:00 Between: 11 (minute)

thickness [of porosity Si]: -- 12 (micrometer)

This substrate was oxidized at 400 ** among oxygen environment for 1 hour. The wall of the hole of porosity Si was covered with this oxidation with the oxidizing film. 1 micrometer grew the single crystal InP epitaxially by the MOCVD (Metal Organic Chemical Vapor Deposition) method on porosity Si.

[0170]pile up after putting this InP surface and the surface of the quartz substrate (the 2nd substrate) prepared independently to nitrogen plasma, respectively -- it was made to contact and annealed 200 ** - 10 h.

[0171]After removing the rear-face oxide film of the 1st substrate, the entire wafer surface was irradiated with CO_2 laser of the about [500-1000W] output from the 1st substrate side. It was absorbed by the InP layer, the temperature of the porous Si layer of the neighborhood rose rapidly, and the rapid heat stress in a lower porous Si layer separated CO_2 laser in the lower porous Si layer. Continuation or a pulse is also available for laser.

[0172]Then, selective etching was carried out, stirring the porous Si layer which remained in the 2nd substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal InP remained without being etched, as a material of an etch stop, selective etching of the porosity Si was carried out, and the single crystal InP was removed thoroughly.

[0173]In this way, the single crystal InP layer which had a thickness of 1 micrometer on the quartz

substrate has been formed. When 100 points were measured for the thickness of the formed single crystal InP layer about the whole surface within a field, the homogeneity of thickness was 1micrometer**29.0nm.

[0174]As a result of the section observation by a transmission electron microscope, a new crystal defect was not introduced into an InP layer, but it was checked that good crystallinity is maintained.

[0175]Selective etching was carried out also stirring after that porosity Si which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single crystal Si remained without being etched, and as a material of an etch stop, selective etching of the porosity Si was carried out, it was removed thoroughly, and was able to supply single crystal Si to the anodization process as the 1st substrate again.

[0176](Example 8) Into the HF solution, anodization was carried out to both sides of the 1st single crystal Si substrate.

[0177]The anodization conditions were as follows. anodization was performed one side every 11.

[0178]

Current density: 7 ($mA\text{-}cm^{-2}$)

Anodization solution: $HF:H_2O:C_2H_5OH$= 1:1:1:00 Between: 11x2 (minute)

thickness [of porosity Si]: -- 12 (micrometer)

This substrate was oxidized at 400 ** among oxygen environment for 1 hour. The wall of the hole of porosity Si was covered with this oxidation with the oxidizing film. 0.15 micrometer grew single crystal Si epitaxially by the CVD (Chemical Vapor Deposition) method on double-sided porosity Si. The growing condition is as follows.

[0179]

Source gas: SiH_2Cl_2/H_2 gas mass flow : 0.5 / 180 l/min gas pressure : 80Torr ** Degree : 950 ** growth rate : To a 0.3 micrometer/min pan. A 100-nm SiO_2 layer was formed in this double-sided epitaxial Si layer surface by thermal oxidation.

[0180]This SiO_2 layer surface and the surface of the Si substrate (the 2nd substrate) of two sheets in which the 500-nm SiO_2 layer prepared independently was formed were piled up, and were contacted.

[0181]After removing the rear-face oxide film of the 2nd two substrates, the entire wafer surface was irradiated with CO_2 laser of the about [500-1000W] output from the 2nd substrate side. It was absorbed by the 500-nm SiO_2 layer of the lamination interface, the temperature of the epitaxial layer of the neighborhood and the porous Si layer rose rapidly, and the rapid heat stress in a lower porous Si layer separated CO_2 laser in the lower porous Si layer. Continuation or a pulse is also available for laser.

[0182]Then, selective etching was carried out, stirring the porous Si layer which remained in the 2nd substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single

crystal Si remained without being etched, as a material of an etch stop, selective etching of the porosity Si was carried out, and single crystal Si was removed thoroughly.

[0183]In this way, the single crystal Si layer which had a thickness of 0.1 micrometer on the Si oxide film has formed two sheets. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 101nm**3nm.

[0184]Furthermore, it heat-treated at 1100 ** in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of a 50-micrometer angle was equivalent to the Si wafer usually marketed at about 0.2 nm.

[0185]As a result of the section observation by a transmission electron microscope, a new crystal defect was not introduced into a Si layer, but it was checked that good crystallinity is maintained.

[0186]The same result was obtained even if it did not form an oxide film in the epitaxial Si layer surface.

[0187]Selective etching was carried out also stirring after that porosity Si which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single crystal Si remained without being etched, and as a material of an etch stop, selective etching of the porosity Si was carried out, it was removed thoroughly, and was able to supply single crystal Si to the oxide film formation process as an anodization process or the 2nd substrate as the 1st substrate again.

[0188](Example 9) A 100-nm SiO_2 layer was formed in the surface of the 1st single crystal Si substrate by thermal oxidation. The hydrogen ion was cm^{-2}[$1x10^{17}$/]-poured into the main table side by accelerating voltage 25keV. Thereby, the porous structure by a hydrogen bubble was formed in the place of the depth near bottom 0.3 micrometer of the surface.

[0189]The SiO_2 layer surface of the 1st Si substrate and the surface of the Si substrate (the 2nd substrate) in which the 500-nm SiO_2 layer prepared independently was formed were piled up, and were contacted.

[0190]After removing the rear-face oxide film of the 1st substrate, the entire wafer surface was irradiated with CO_2 laser of the about [500-1000W] output from the 1st substrate side. It was absorbed by the 500-nm SiO_2 layer of the lamination interface, the temperature of the epitaxial layer of the neighborhood and the porous Si layer rose rapidly, and the rapid heat stress in a lower porous Si layer separated CO_2 laser in the lower porous Si layer. Continuation or a pulse is also available for laser.

[0191]Then, selective etching was carried out, stirring the porous Si layer which remained in the 2nd substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single crystal Si remained without being etched, as a material of an etch stop, selective etching of the porosity Si was carried out, and single crystal Si was removed thoroughly.

[0192]That is, the single crystal Si layer which had a thickness of 0.1 micrometer on the Si oxide film

has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 101nm**3nm.
[0193]Furthermore, it heat-treated at 1100 ** in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of a 50-micrometer angle was equivalent to the Si wafer usually marketed at about 0.2 nm.
[0194]As a result of the section observation by a transmission electron microscope, a new crystal defect was not introduced into a Si layer, but it was checked that good crystallinity is maintained.
[0195]The same result was obtained even if it did not form an oxide film in the epitaxial Si layer surface.
[0196]Selective etching is carried out also stirring after that porosity Si which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single crystal Si remained without being etched, and as a material of an etch stop, selective etching of the porosity Si was carried out, it was removed thoroughly, and was able to supply single crystal Si to the oxide film formation process as an anodization process or the 2nd substrate as the 1st substrate again.
[0197](Example 10) Into the HF solution, anodization was performed to the surface layer of the 1st single crystal Si substrate.
[0198]The anodization conditions were as follows.
[0199]

Current density: 7 ($mA\text{-}cm^{-2}$)
Anodization solution: $HF:H_2O:C_2H_5OH$= 1:1:1:00 Between: 11 (minute)

thickness [of porosity Si]: -- 12 (micrometer)
This substrate was oxidized at 400 ** among oxygen environment for 1 hour. The wall of the hole of porosity Si was covered with this oxidation with the oxidizing film. 0.15 micrometer grew single crystal Si epitaxially by the CVD (Chemical Vapor Deposition) method on porosity Si. The growing condition is as follows.
[0200]
Source gas: SiH_2Cl_2/H_2 gas mass flow : 0.5 / 180 l/min gas pressure : 80Torr ** Degree : 950 **

growth rate : To a 0.3 micrometer/min pan. A 100-nm SiO_2 layer was formed in this epitaxial Si layer surface by thermal oxidation.

[0201]The hydrogen ion was cm^{-2}[$5x10^{16}$/]-poured into the main table side by accelerating voltage 180keV.
[0202]This SiO_2 layer surface and the surface of the Si substrate (the 2nd substrate) in which the 500-nm SiO_2 layer prepared independently was formed were piled up, and were contacted.

[0203]After removing the rear-face oxide film of the 1st substrate, the entire wafer surface was irradiated with CO_2 laser of the about [500-1000W] output from the 1st substrate side. It was absorbed by the 500-nm SiO_2 layer of the lamination interface, the temperature of the epitaxial layer

of the neighborhood and the porous Si layer rose rapidly, and the rapid heat stress in a lower porous Si layer separated CO_2 laser in the lower porous Si layer. Continuation or a pulse is also available for laser. The separating position was mostly controlled by the ion implantation, and it dissociated from the SiO_2 surface in front of lamination in the porous Si layer of a place of about 1.5 micrometers.

[0204]Then, selective etching was carried out, stirring the porous Si layer which remained in the 2nd substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single crystal Si remained without being etched, as a material of an etch stop, selective etching of the porosity Si was carried out, and single crystal Si was removed thoroughly.

[0205]Thereby, the single crystal Si layer which had a thickness of 0.1 micrometer on the Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 101nm**3nm.

[0206]Furthermore, it heat-treated at 1100 ** in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of a 50-micrometer angle was equivalent to the Si wafer usually marketed at about 0.2 nm.

[0207]As a result of the section observation by a transmission electron microscope, a new crystal defect was not introduced into a Si layer, but it was checked that good crystallinity is maintained.

[0208]The same result was obtained even if it did not form an oxide film in the epitaxial Si layer surface.

[0209]Selective etching was carried out also stirring after that porosity Si which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single crystal Si remained without being etched, and as a material of an etch stop, selective etching of the porosity Si was carried out, it was removed thoroughly, and was able to supply single crystal Si to the oxide film formation process as an anodization process or the 2nd substrate as the 1st substrate again.

[0210](Example 11) Into the HF solution, anodization was performed to the surface layer of the 1st single crystal Si substrate.

[0211]The anodization conditions were as follows.

[0212]

Current density: 7 ($mA\text{-}cm^{-2}$)

Anodization solution: $HF:H_2O:C_2H_5OH$= 1:1:1:00 Between: 11 (minute)

thickness [of porosity Si]: -- 12 (micrometer)

This substrate was oxidized at 400 ** among oxygen environment for 1 hour. The wall of the hole of porosity Si was covered with this oxidation with the oxidizing film. 0.15 micrometer grew single crystal Si epitaxially by the CVD (Chemical Vapor Deposition) method on porosity Si. The growing condition is as follows.

[0213]

Source gas: SiH_2Cl_2/H_2 gas mass flow : 0.5 / 180 l/min gas pressure : 80Torr ** Degree : 950 **

growth rate : To a 0.3 micrometer/min pan. A 100-nm SiO_2 layer was formed in this epitaxial Si layer surface by thermal oxidation.

[0214]This SiO_2 layer surface and the surface of the Si substrate (the 2nd substrate) prepared independently were piled up, and were contacted.

[0215]After removing the rear-face oxide film of the 1st substrate, the entire wafer surface was irradiated with CO_2 laser of the about [500-1000W] output from the 1st substrate side. It was absorbed by the 500-nm SiO_2 layer of the lamination interface, the temperature of the epitaxial layer of the neighborhood and the porous Si layer rose rapidly, and the rapid heat stress in a lower porous Si layer separated CO_2 laser in the lower porous Si layer. Continuation or a pulse is also available for laser.

[0216]Then, selective etching was carried out, stirring the porous Si layer which remained in the 2nd substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single crystal Si remained without being etched, as a material of an etch stop, selective etching of the porosity Si was carried out, and single crystal Si was removed thoroughly.

[0217]In this way, the single crystal Si layer which had a thickness of 0.1 micrometer on the Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 101nm**3nm.

[0218]Furthermore, it heat-treated at 1100 ** in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of a 50-micrometer angle was equivalent to the Si wafer usually marketed at about 0.2 nm.

[0219]As a result of the section observation by a transmission electron microscope, a new crystal defect was not introduced into a Si layer, but it was checked that good crystallinity is maintained.

[0220]Selective etching is carried out also stirring after that porosity Si which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single crystal Si remained without being etched, as a material of an etch stop, selective etching was able to be carried out, it was able to be removed thoroughly, single crystal Si was able to be again pasted together as an anodization process or the 2nd substrate as the 1st substrate, and porosity Si was able to supply it to the process.

[0221](Example 12) Into the HF solution, anodization was performed to the surface layer of the 1st single crystal Si substrate.

[0222]The anodization conditions were as follows.

[0223]

Current density: 7 ($mA\text{-}cm^{-2}$)

Anodization solution: $HF:H_2O:C_2H_5OH$= 1:1:1:00 Between: 5.5 (minute)

thickness [of porosity Si]: -- six (micrometer)

Furthermore, it is current density. : 70 ($mA\text{-}cm^{-2}$)

Anodization solution: $HF:H_2O:C_2H_5OH$= 1:1:1:00 Between: 0.5 (minute)

thickness [of porosity Si]: -- five (micrometer)
This substrate was oxidized at 400 ** among oxygen environment for 1 hour. The wall of the hole of porosity Si was covered with this oxidation with the oxidizing film. 0.15 micrometer grew single crystal Si epitaxially by the CVD (Chemical Vapor Deposition) method on porosity Si. The growing condition is as follows.
[0224]
Source gas: SiH_2Cl_2/H_2 gas mass flow : 0.5 / 180 l/min gas pressure : 80Torr ** Degree : 950 ** growth rate : To a 0.3 micrometer/min pan. A 100-nm SiO_2 layer was formed in this epitaxial Si layer surface by thermal oxidation.
[0225]This SiO_2 layer surface and the surface of the Si substrate (the 2nd substrate) prepared independently were piled up, and were contacted.
[0226]After removing the rear-face oxide film of the 1st substrate, the entire wafer surface was irradiated with CO_2 laser of the about [500-1000W] output from the 1st substrate side. It was absorbed by the 500-nm SiO_2 layer of the lamination interface, the temperature of the epitaxial layer of the neighborhood and the porous Si layer rose rapidly, and the rapid heat stress in a lower porous Si layer separated CO_2 laser in the lower porous Si layer. Continuation or a pulse is also available for laser.
[0227]Then, selective etching was carried out, stirring the porous Si layer which remained in the 2nd substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single crystal Si remained without being etched, as a material of an etch stop, selective etching of the porosity Si was carried out, and single crystal Si was removed thoroughly.
[0228]That is, the single crystal Si layer which had a thickness of 0.1 micrometer on the Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 101nm**3nm.
[0229]Furthermore, it heat-treated at 1100 ** in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of a 50-micrometer angle was equivalent to the Si wafer usually marketed at about 0.2 nm.
[0230]As a result of the section observation by a transmission electron microscope, a new crystal defect was not introduced into a Si layer, but it was checked that good crystallinity is maintained.
[0231]Selective etching is carried out also stirring after that porosity Si which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single crystal Si remained without being etched, as a material of an etch stop, selective etching was able to be carried out, it was able to be removed thoroughly, single crystal Si was able to be again pasted together as an anodization process or the 2nd substrate as the 1st substrate, and porosity Si was able to supply it to the process.
[0232](Example 13) Into the HF solution, anodization was performed to the surface layer of the 1st single crystal Si substrate.

[0233]The anodization conditions were as follows.
[0234]

Current density: 7 (mA-cm^{-2})
Anodization solution: HF:H_2O:C_2H_5OH= 1:1:1:00 Between: 3.5 (minute)

thickness [of porosity Si]: -- four (micrometer)

further -- current density: 100 (mA-cm^{-2})
Anodization solution: HF:H_2O:C_2H_5OH= 1:1:1:00 Between: 0.2 (minute)

thickness [of porosity Si]: -- three (micrometer)

Furthermore, it is current density. : 7 (mA-cm^{-2})
Anodization solution: HF:H_2O:C_2H_5OH= 1:1:1:00 Between: 3.5 (minute)

thickness [of porosity Si]: -- four (micrometer)
This substrate was oxidized at 400 ** among oxygen environment for 1 hour. The wall of the hole of porosity Si was covered with this oxidation with the oxidizing film. 0.15 micrometer grew single crystal Si epitaxially by the CVD (Chemical Vapor Deposition) method on porosity Si. The growing condition is as follows.
[0235]
Source gas: SiH_2Cl_2/H_2 gas mass flow : 0.5 / 180 l/min gas pressure : 80Torr ** Degree : 950 ** growth rate : To a 0.3 micrometer/min pan. A 100-nm SiO_2 layer was formed in this epitaxial Si layer surface by thermal oxidation.
[0236]This SiO_2 layer surface and the surface of the Si substrate (the 2nd substrate) prepared independently were piled up, and were contacted.
[0237]After removing the rear-face oxide film of the 1st substrate, the entire wafer surface was irradiated with CO_2 laser of the about [500-1000W] output from the 1st substrate side. It was absorbed by the 500-nm SiO_2 layer of the lamination interface, the temperature of the epitaxial layer of the neighborhood and the porous Si layer rose rapidly, and the rapid heat stress in a middle porous Si layer separated CO_2 laser in the middle porous Si layer. Continuation or a pulse is also available for laser.
[0238]Then, selective etching was carried out, stirring the porous Si layer which remained in the 2nd substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single crystal Si remained without being etched, as a material of an etch stop, selective etching of the porosity Si was carried out, and single crystal Si was removed thoroughly.
[0239]In this way, the single crystal Si layer which had a thickness of 0.1 micrometer on the Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 101nm**3nm.
[0240]Furthermore, it heat-treated at 1100 ** in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of a

50-micrometer angle was equivalent to the Si wafer usually marketed at about 0.2 nm.
[0241]As a result of the section observation by a transmission electron microscope, a new crystal defect was not introduced into a Si layer, but it was checked that good crystallinity is maintained.
[0242]Selective etching is carried out also stirring after that porosity Si which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single crystal Si remained without being etched, as a material of an etch stop, selective etching was able to be carried out, it was able to be removed thoroughly, single crystal Si was able to be again pasted together as an anodization process or the 2nd substrate as the 1st substrate, and porosity Si was able to supply it to the process.
[0243](Example 14) Into the HF solution, anodization was performed to the surface layer of the 1st single crystal Si substrate.
[0244]The anodization conditions were as follows.
[0245]

Current density: 7 ($mA\text{-}cm^{-2}$)
Anodization solution: $HF:H_2O:C_2H_5OH$= 1:1:1:00 Between: 11 (minute)

thickness [of porosity Si]: -- 12 (micrometer)
This substrate was oxidized at 400 ** among oxygen environment for 1 hour. The wall of the hole of porosity Si was covered with this oxidation with the oxidizing film. 0.15 micrometer grew single crystal Si epitaxially by the CVD (Chemical Vapor Deposition) method on porosity Si. The growing condition is as follows.
[0246]

Source gas: SiH_2Cl_2/H_2 gas mass flow : 0.5 / 180 l/min gas pressure : 80Torr ** Degree : 950 **

growth rate : To a 0.3 micrometer/min pan. A 100-nm SiO_2 layer was formed in this epitaxial Si layer surface by thermal oxidation.
[0247]This SiO_2 layer surface and the surface of the Si substrate (the 2nd substrate) prepared independently were piled up, and were contacted.
[0248]Then, the lamination base was heated at about 1250 ** with the heat treating furnace. The rapid heat stress of the porous Si layer separated in the porous Si layer. Heat treatment may be added in order to raise lamination intensity.
[0249]Then, selective etching was carried out, stirring the porous Si layer which remained in the 2nd substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single crystal Si remained without being etched, as a material of an etch stop, selective etching of the porosity Si was carried out, and single crystal Si was removed thoroughly.
[0250]In this way, the single crystal Si layer which had a thickness of 0.1 micrometer on the Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 101nm**3nm.
[0251]Furthermore, it heat-treated at 1100 ** in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of a

50-micrometer angle was equivalent to the Si wafer usually marketed at about 0.2 nm.
[0252]As a result of the section observation by a transmission electron microscope, a new crystal defect was not introduced into a Si layer, but it was checked that good crystallinity is maintained.
[0253]The same result was obtained even if it did not form an oxide film in the epitaxial Si layer surface.
[0254]Selective etching is carried out also stirring after that porosity Si which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single crystal Si remained without being etched, as a material of an etch stop, selective etching was able to be carried out, it was able to be removed thoroughly, single crystal Si was able to be again pasted together as an anodization process or the 2nd substrate as the 1st substrate, and porosity Si was able to supply it to the process.
[0255](Example 15) Into the HF solution, anodization was performed to the surface layer of the 1st single crystal Si substrate.
[0256]The anodization conditions were as follows.
[0257]

Current density: 7 ($mA\text{-}cm^{-2}$)
Anodization solution: $HF:H_2O:C_2H_5OH$= 1:1:1:00 Between: 11 (minute)

thickness [of porosity Si]: -- 12 (micrometer)
This substrate was oxidized at 400 ** among oxygen environment for 1 hour. The wall of the hole of porosity Si was covered with this oxidation with the oxidizing film. 0.15 micrometer grew single crystal Si epitaxially by the CVD (Chemical Vapor Deposition) method on porosity Si. The growing condition is as follows.
[0258]
Source gas: SiH_2Cl_2/H_2 gas mass flow : 0.5 / 180 l/min gas pressure : 80Torr ** Degree : 950 **

growth rate : To a 0.3 micrometer/min pan. A 100-nm SiO_2 layer was formed in this epitaxial Si layer surface by thermal oxidation.
[0259]This SiO_2 layer surface and the surface of the Si substrate (the 2nd substrate) in which the 500-nm SiO_2 layer prepared independently was formed were piled up, and were contacted.
[0260]Then, the lamination base was heated at about 1250 ** with the heat treating furnace. The rapid heat stress of the porous Si layer separated in the porous Si layer. Heat treatment may be added in order to raise lamination intensity.
[0261]Then, selective etching was carried out, stirring the porous Si layer which remained in the 2nd substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single crystal Si remained without being etched, as a material of an etch stop, selective etching of the porosity Si was carried out, and single crystal Si was removed thoroughly.
[0262]In this way, the single crystal Si layer which had a thickness of 0.1 micrometer on the Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal

Si layer about the whole surface within a field, the homogeneity of thickness was 101nm**3nm.
[0263]Furthermore, it heat-treated at 1100 ** in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of a 50-micrometer angle was equivalent to the Si wafer usually marketed at about 0.2 nm.
[0264]As a result of the section observation by a transmission electron microscope, a new crystal defect was not introduced into a Si layer, but it was checked that good crystallinity is maintained.
[0265]The same result was obtained even if it did not form an oxide film in the epitaxial Si layer surface.
[0266]Selective etching was carried out also stirring after that porosity Si which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single crystal Si remained without being etched, and as a material of an etch stop, selective etching of the porosity Si was carried out, it was removed thoroughly, and was able to supply single crystal Si to the oxide film formation process as an anodization process or the 2nd substrate as the 1st substrate again.
[0267](Example 16) Into the HF solution, anodization was performed to the surface layer of the 1st single crystal Si substrate.
[0268]The anodization conditions were as follows.
[0269]

Current density: 7 ($mA\text{-}cm^{-2}$)
Anodization solution: $HF:H_2O:C_2H_5OH$= 1:1:1:00 Between: 3.5 (minute)

thickness [of porosity Si]: -- four (micrometer)

further -- current density: 100 ($mA\text{-}cm^{-2}$)
Anodization solution: $HF:H_2O:C_2H_5OH$= 1:1:1:00 Between: 0.2 (minute)

thickness [of porosity Si]: -- three (micrometer)

further -- current density: 7 ($mA\text{-}cm^{-2}$)
Anodization solution: $HF:H_2O:C_2H_5OH$= 1:1:1:00 Between: 3.5 (minute)

thickness [of porosity Si]: -- four (micrometer)
This substrate was oxidized at 400 ** among oxygen environment for 1 hour. The wall of the hole of porosity Si was covered with this oxidation with the oxidizing film. 0.15 micrometer grew single crystal Si epitaxially by the CVD (Chemical Vapor Deposition) method on porosity Si. The growing condition is as follows.
[0270]
Source gas: SiH_2Cl_2/H_2 gas mass flow : 0.5 / 180 l/min gas pressure : 80Torr ** Degree : 950 **

growth rate : To a 0.3 micrometer/min pan. A 100-nm SiO_2 layer was formed in this epitaxial Si layer surface by thermal oxidation.
[0271]This SiO_2 layer surface and the surface of the Si substrate (the 2nd substrate) prepared independently were piled up, and were contacted.

[0272]Then, the lamination base was heated at about 600-1200 ** with the heat treating furnace. The rapid heat stress of the porous Si layer separated in the porous Si layer. Heat treatment may be added in order to raise lamination intensity.
[0273]Then, selective etching was carried out, stirring the porous Si layer which remained in the 2nd substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single crystal Si remained without being etched, as a material of an etch stop, selective etching of the porosity Si was carried out, and single crystal Si was removed thoroughly.
[0274]That is, the single crystal Si layer which had a thickness of 0.1 micrometer on the Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 101nm**3nm.
[0275]Furthermore, it heat-treated at 1100 ** in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of a 50-micrometer angle was equivalent to the Si wafer usually marketed at about 0.2 nm.
[0276]As a result of the section observation by a transmission electron microscope, a new crystal defect was not introduced into a Si layer, but it was checked that good crystallinity is maintained.
[0277]Selective etching is carried out also stirring after that porosity Si which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single crystal Si remained without being etched, as a material of an etch stop, selective etching was able to be carried out, it was able to be removed thoroughly, single crystal Si was able to be again pasted together as an anodization process or the 2nd substrate as the 1st substrate, and porosity Si was able to supply it to the process.
[0278](Example 17) Into the HF solution, anodization was performed to the surface layer of the 1st single crystal Si substrate.
[0279]The anodization conditions were as follows.
[0280]

Current density: 7 ($mA\text{-}cm^{-2}$)
Anodization solution: $HF:H_2O:C_2H_5OH$= 1:1:1:00 Between: 5.5 (minute)

thickness [of porosity Si]: -- six (micrometer)

Furthermore, it is current density. : 70 ($mA\text{-}cm^{-2}$)
Anodization solution: $HF:H_2O:C_2H_5OH$= 1:1:1:00 Between: 0.5 (minute)

thickness [of porosity Si]: -- five (micrometer)
This substrate was oxidized at 400 ** among oxygen environment for 1 hour. The wall of the hole of porosity Si was covered with this oxidation with the thin oxidizing film.
[0281]Subsequently, the thin oxide film which dipped the near outermost surface in which the porous layer of this substrate was formed in 1.25% of HF solution, and was formed in the outermost surface was removed. In this way, heat treatment for 1 minute was performed for H_2 to the obtained substrate on condition of 1050 ** and 760Torr with 230 l. / min sink this time, and heat treatment for 5 minutes

was performed on the conditions which carried out 50sccm addition of the SiH_4 further.

[0282]Subsequently, 0.15 micrometer grew single crystal Si epitaxially by the CVD (Chemical Vapor Deposition) method on the porous Si layer. The growing condition is as follows.

[0283]

Source gas: SiH_2Cl_2/H_2 gas mass flow : 0.5 / 180 l/min gas pressure : 80Torr ** Degree : 950 ** growth rate : To a 0.3 micrometer/min pan. A 100-nm SiO_2 layer was formed in this epitaxial Si layer surface by thermal oxidation.

[0284]This SiO_2 layer surface and the surface of the Si substrate (the 2nd substrate) prepared independently were piled up, and were contacted.

[0285]After removing the rear-face oxide film of the 1st substrate, the entire wafer surface was irradiated with CO_2 laser of the about [500-1000W] output from the 1st substrate side. It was absorbed by the 500-nm SiO_2 layer of the lamination interface, the temperature of the epitaxial layer of the neighborhood and the porous Si layer rose rapidly, and the rapid heat stress in a lower porous Si layer separated CO_2 laser in the lower porous Si layer. Continuation or a pulse is also available for laser.

[0286]Then, selective etching was carried out, stirring the porous Si layer which remained in the 2nd substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single crystal Si remained without being etched, as a material of an etch stop, selective etching of the porosity Si was carried out, and single crystal Si was removed thoroughly.

[0287]That is, the single crystal Si layer which had a thickness of 0.1 micrometer on the Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 101nm**3nm.

[0288]Furthermore, it heat-treated at 1100 ** in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of a 50-micrometer angle was equivalent to the Si wafer usually marketed at about 0.2 nm.

[0289]As a result of the section observation by a transmission electron microscope, a new crystal defect was not introduced into a Si layer, but it was checked that good crystallinity is maintained.

[0290]Selective etching is carried out also stirring after that porosity Si which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Single crystal Si remained without being etched, as a material of an etch stop, selective etching was able to be carried out, it was able to be removed thoroughly, single crystal Si was able to be again pasted together as an anodization process or the 2nd substrate as the 1st substrate, and porosity Si was able to supply it to the process.

[Translation done.]

* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1]A process of preparing the 1st base in which a nonvesicular semiconductor layer was allotted on said porous silicon layer of a silicon substrate which has a porous silicon layer, A process of pasting said 1st base and the 2nd base together so that a multilayer-structure object in which said nonvesicular semiconductor layer is located inside may be acquired, A manufacturing method of a semiconductor member having a process of separating said multilayer-structure object in said porous silicon layer by heating said multilayer-structure object, and the process of removing a porous silicon layer which remained in said separated 2nd base side.
[Claim 2]A process of preparing the 1st base in which a nonvesicular semiconductor layer was allotted on said porous silicon layer of a silicon substrate which has a porous silicon layer, A process of pasting said 1st base and the 2nd base together so that a multilayer-structure object in which said nonvesicular semiconductor layer is located inside may be acquired, A process of separating said multilayer-structure object in said porous silicon layer by heating said multilayer-structure object, A manufacturing method of a semiconductor member having a process of removing a porous silicon layer which remained in said separated 2nd base side, and the process of using a base produced by removing a porous silicon layer which remained in said separated 1st base side as raw material material of said 1st base.
[Claim 3]A process of preparing the 1st base in which a nonvesicular semiconductor layer was allotted on said porous silicon layer of a silicon substrate which has a porous silicon layer, A process of pasting said 1st base and the 2nd base together so that a multilayer-structure object in which said nonvesicular semiconductor layer is located inside may be acquired, A process of separating said multilayer-structure object in said porous silicon layer by heating said multilayer-structure object, A manufacturing method of a semiconductor member having a process of removing a porous silicon layer which remained in said separated 2nd base side, and the process of using a base produced by removing a porous silicon layer which remained in said separated 1st base side as raw material material of said 2nd base.
[Claim 4]A manufacturing method of the semiconductor member according to any one of claims 1 to 3

which performs said heating using a heat treating furnace.
[Claim 5]A manufacturing method of the semiconductor member according to any one of claims 1 to 3 in which said heating is what heats said multilayer-structure object selectively.
[Claim 6]A manufacturing method of the semiconductor member according to claim 5 by which said heating is made by laser radiation.
[Claim 7]A manufacturing method of the semiconductor member according to claim 6 in which said laser is carbon dioxide laser.
[Claim 8]A manufacturing method of the semiconductor member according to claim 5 made when said heating sends current through said porous silicon layer.
[Claim 9]A manufacturing method of the semiconductor member according to any one of claims 1 to 3 which forms said nonvesicular semiconductor layer on this 2 ** porous silicon layer after forming said porous silicon layer in two fields of said silicon substrate.
[Claim 10]A manufacturing method of the semiconductor member according to any one of claims 1 to 3 produced by said porous silicon layer giving anodization to said silicon substrate.
[Claim 11]Said 1st base is carrying out the ion implantation of the element chosen from rare gas, hydrogen, and nitrogen to said silicon substrate, A manufacturing method of the semiconductor member according to any one of claims 1 to 3 which makes an ion implantation region of a certain depth said porous silicon layer from the surface of a silicon substrate, and is constituted considering a surface layer as said nonvesicular semiconductor layer.
[Claim 12]A manufacturing method of the semiconductor member according to any one of claims 1 to 3 constituted by forming said nonvesicular semiconductor layer on this porous silicon layer after said 1st base forms said porous silicon layer into said silicon substrate.
[Claim 13]A manufacturing method of the semiconductor member according to any one of claims 1 to 3 with which said nonvesicular semiconductor layer comprises a single crystal silicon layer.
[Claim 14]A manufacturing method of the semiconductor member according to claim 13 with which said single crystal silicon layer is formed by epitaxial growth.
[Claim 15]A manufacturing method of the semiconductor member according to claim 13 which a silicon oxide layer is formed in the surface of said single crystal silicon layer, and constitutes said 1st base.
[Claim 16]A manufacturing method of the semiconductor member according to claim 15 with which said silicon oxide layer is formed of thermal oxidation.
[Claim 17]A manufacturing method of the semiconductor member according to any one of claims 1 to 3 with which said porosity semiconductor layer comprises a compound semiconductor layer.
[Claim 18]A manufacturing method of the semiconductor member according to claim 17 with which said compound semiconductor layer constitutes a single crystal.
[Claim 19]A manufacturing method of the semiconductor member according to any one of claims 1 to 3 using a single crystal silicon substrate as said 2nd base.
[Claim 20]A manufacturing method of the semiconductor member according to any one of claims 1 to 3 using a substrate which formed an oxide film on the surface of a single crystal silicon substrate as

said 2nd base.

[Claim 21]A manufacturing method of the semiconductor member according to any one of claims 1 to 3 using a light transmittance state base as said 2nd base.

[Claim 22]A manufacturing method of the semiconductor member according to claim 21 which uses a glass substrate for said light transmittance state base.

[Claim 23]A manufacturing method of the semiconductor member according to any one of claims 1 to 3 made when said lamination process sticks two bases.

[Claim 24]A manufacturing method of the semiconductor member according to any one of claims 1 to 3 with which said lamination process is made using anode joining, application of pressure, and heat treatment.

[Claim 25]A manufacturing method of the semiconductor member according to any one of claims 1 to 3 with which removal of said porous silicon layer is made by polish.

[Claim 26]A manufacturing method of the semiconductor member according to any one of claims 1 to 3 by which removal of said porous silicon layer is made by etching.

[Claim 27]A manufacturing method of the semiconductor member according to claim 26 with which said etching is made using fluoric acid.

[Claim 28]A semiconductor member manufactured by the manufacturing method according to any one of claims 1 to 27.

[Translation done.]

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CORRECTION OR AMENDMENT

[Kind of official gazette]Printing of amendment by regulation of 2 of Article 17 of Patent Law
[Section classification] The 2nd classification of the part VII gate
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21/02 B

21/20
[Written amendment]
[Filing date]March 4, Heisei 11
[Amendment 1]
[Document to be Amended]Specification
[Item(s) to be Amended]Claim
[Method of Amendment]Change
[Proposed Amendment]
[Claim(s)]
[Claim 1]A process of preparing the 1st base that has a nonvesicular semiconductor layer via a porous silicon layer on a silicon substrate,

A process of pasting said 1st base and the 2nd base together so that a multilayer-structure object in which said nonvesicular semiconductor layer is located inside may be acquired,
A partition process which separates said multilayer-structure object in said porous silicon layer by heating said multilayer-structure object,
A manufacturing method of a semiconductor member having the process of removing porous silicon which remained in said separated 2nd base side.
[Claim 2]A process of preparing the 1st base that has a nonvesicular semiconductor layer via a porous silicon layer on a silicon substrate,
A process of pasting said 1st base and the 2nd base together so that a multilayer-structure object in which said nonvesicular semiconductor layer is located inside may be acquired,
A partition process which separates said multilayer-structure object in said porous silicon layer by heating selectively said porous silicon layer and/or said neighborhood of a porous silicon layer,
A manufacturing method of a semiconductor member having the process of removing porous silicon which remained in said separated 2nd base side.
[Claim 3]A manufacturing method of the semiconductor member according to claim 1 or 2 which has the process of using a base produced by removing a porous silicon layer which remained in the separated 1st [said] base side after said partition process as raw material of said 1st base.
[Claim 4]A manufacturing method of the semiconductor member according to claim 1 or 2 which has the process of using a base produced by removing a porous silicon layer which remained in the separated 1st [said] base side after said partition process as raw material of said 2nd base.
[Claim 5]A manufacturing method of the semiconductor member according to any one of claims 1 to 4 which performs said heating using a heat treating furnace.
[Claim 6]A manufacturing method of the semiconductor member according to any one of claims 1 to 4 by which said heating is made by laser radiation.
[Claim 7]A manufacturing method of the semiconductor member according to claim 6 in which said laser is carbon dioxide laser.
[Claim 8]A manufacturing method of the semiconductor member according to any one of claims 1 to 4 made when said heating sends current through said porous silicon layer or its neighborhood.
[Claim 9]A manufacturing method of the semiconductor member according to claim 1 or 2 made when said heating sends current through said nonvesicular semiconductor layer.
[Claim 10]A manufacturing method of the semiconductor member according to claim 1 or 2 which forms said nonvesicular semiconductor layer on this 2 ** porous silicon layer after forming said porous silicon layer in two fields of said silicon substrate.
[Claim 11]A manufacturing method of the semiconductor member according to claim 1 or 2 produced by said porous silicon layer giving anodization to said silicon substrate.
[Claim 12]A manufacturing method of the semiconductor member according to claim 1 or 2 with which said porous silicon layer consists of the 2nd porous silicon layer from said silicon substrate side whose porosity is smaller than the 1st porous silicon layer and said 1st porous silicon layer.
[Claim 13]Said porous silicon layer From said silicon substrate side to the 1st porous silicon layer. A

manufacturing method of the semiconductor member according to claim 1 or 2 which consists of the 2nd porous silicon layer with larger porosity than said 1st porous silicon layer, and the 3rd porous silicon layer whose porosity is smaller than said 2nd porous silicon layer.

[Claim 14]Said 1st base is carrying out the ion implantation of the element chosen from rare gas, hydrogen, and nitrogen to said silicon substrate, A manufacturing method of the semiconductor member according to claim 1 or 2 which makes an ion implantation region of a certain depth said porous silicon layer from the surface of a silicon substrate, and is constituted considering a surface layer as said nonvesicular semiconductor layer.

[Claim 15]A manufacturing method of the semiconductor member according to claim 1 or 2 constituted by forming said nonvesicular semiconductor layer on this porous silicon layer after said 1st base forms said porous silicon layer into said silicon substrate.

[Claim 16]A manufacturing method of the semiconductor member according to claim 1 or 2 with which said nonvesicular semiconductor layer comprises a single crystal silicon layer.

[Claim 17]A manufacturing method of the semiconductor member according to claim 16 with which said single crystal silicon layer is formed by epitaxial growth.

[Claim 18]A manufacturing method of the semiconductor member according to claim 16 which a silicon oxide layer is formed in the surface of said single crystal silicon layer, and constitutes said 1st base.

[Claim 19]A manufacturing method of the semiconductor member according to claim 18 with which said silicon oxide layer is formed of thermal oxidation.

[Claim 20]A manufacturing method of the semiconductor member according to claim 1 or 2 with which said porosity semiconductor layer comprises a compound semiconductor layer.

[Claim 21]A manufacturing method of the semiconductor member according to claim 20 with which said compound semiconductor layer constitutes a single crystal.

[Claim 22]A manufacturing method of the semiconductor member according to claim 1 or 2 with which said nonvesicular semiconductor layer consists of polycrystal Si, amorphous Si, GaAS, InP, GaAsP, GaAlAs, InAs, AlGaSb, InGaAs, ZnS, CdSe, CdTe, or SiGe.

[Claim 23]A manufacturing method of the semiconductor member according to claim 1 or 2 using a single crystal silicon substrate as said 2nd base.

[Claim 24]A manufacturing method of the semiconductor member according to claim 1 or 2 using a substrate which formed an oxide film on the surface of a single crystal silicon substrate as said 2nd base.

[Claim 25]A manufacturing method of the semiconductor member according to claim 1 or 2 using a light transmittance state base as said 2nd base.

[Claim 26]A manufacturing method of the semiconductor member according to claim 25 which uses a glass substrate for said light transmittance state base.

[Claim 27]A manufacturing method of the semiconductor member according to claim 1 or 2 made when said lamination process sticks two bases.

[Claim 28]A manufacturing method of the semiconductor member according to claim 1 or 2 with which

said lamination process is made using anode joining, application of pressure, and heat treatment.
[Claim 29]A manufacturing method of the semiconductor member according to claim 1 or 2 with which removal of said porous silicon layer is made by polish.
[Claim 30]A manufacturing method of the semiconductor member according to claim 1 or 2 by which removal of said porous silicon layer is made by etching.
[Claim 31]A manufacturing method of the semiconductor member according to claim 30 with which said etching is made using fluoric acid.
[Claim 32]A manufacturing method of the semiconductor member according to claim 1 or 2 obtained by forming said nonvesicular semiconductor layer after said 1st base forms an oxide film in a wall of a hole of said porous silicon layer.
[Claim 33]Claims 1 and 2 obtained by forming said nonvesicular semiconductor layer after said 1st base heat-treats said porous silicon layer in atmosphere containing hydrogen, or a manufacturing method of a semiconductor member given in 32.
[Claim 34]Claims 1, 2, and 32 which have the process of heat-treating said nonvesicular semiconductor layer in atmosphere containing hydrogen, after said partition process, or a manufacturing method of a semiconductor member given in 33.
[Claim 35]A manufacturing method of the semiconductor member according to claim 1 or 2 which is a process heated without said partition process's oxidizing.
[Claim 36]A semiconductor member manufactured by the manufacturing method according to any one of claims 1 to 35.
[The amendment 2]
[Document to be Amended]Specification
[Item(s) to be Amended]0043
[Method of Amendment]Change
[Proposed Amendment]
[0043]
[Means for Solving the Problem]A process for which a manufacturing method of a semiconductor member of this invention prepares the 1st base that has a nonvesicular semiconductor layer via a porous silicon layer on a silicon substrate, A process of pasting said 1st base and the 2nd base together so that a multilayer-structure object in which said nonvesicular semiconductor layer is located inside may be acquired, It has a partition process which separates said multilayer-structure object in said porous silicon layer, and the process of removing porous silicon which remained in said separated 2nd base side, by heating said multilayer-structure object.
[Amendment 3]
[Document to be Amended]Specification
[Item(s) to be Amended]0044
[Method of Amendment]Change
[Proposed Amendment]
[0044]The process for which the manufacturing method of the semiconductor member of this

invention prepares the 1st base that has a nonvesicular semiconductor layer via a porous silicon layer on a silicon substrate, The process of pasting said 1st base and the 2nd base together so that the multilayer-structure object in which said nonvesicular semiconductor layer is located inside may be acquired, It has a partition process which separates said multilayer-structure object in said porous silicon layer, and the process of removing the porous silicon which remained in said separated 2nd base side, by heating selectively said porous silicon layer and/or said neighborhood of a porous silicon layer.

[Amendment 4]

[Document to be Amended]Specification

[Item(s) to be Amended]0045

[Method of Amendment]Deletion

[Translation done.]